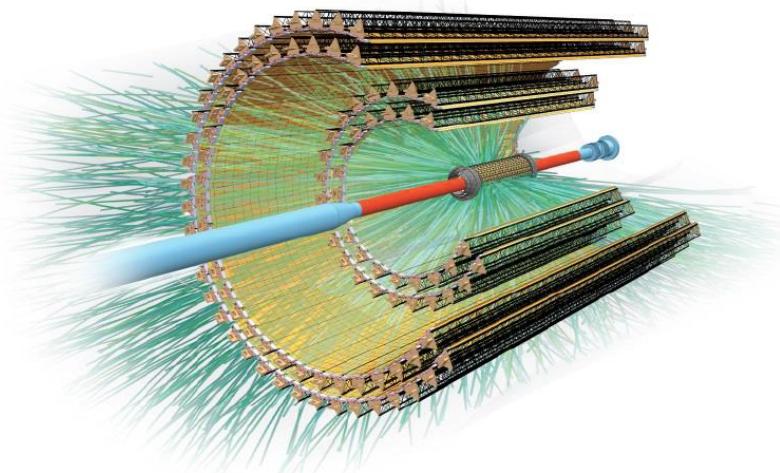


# Upgrade of the ALICE Silicon Tracker Using CMOS Pixel Sensors

Luciano Musa - CERN



*sPHENIX MAPS Cost & Schedule Workfest*  
31 March 2016

# Upgrade of the ALICE Silicon Tracker Using CMOS Pixel Sensors

A Large Ion Collider Experiment



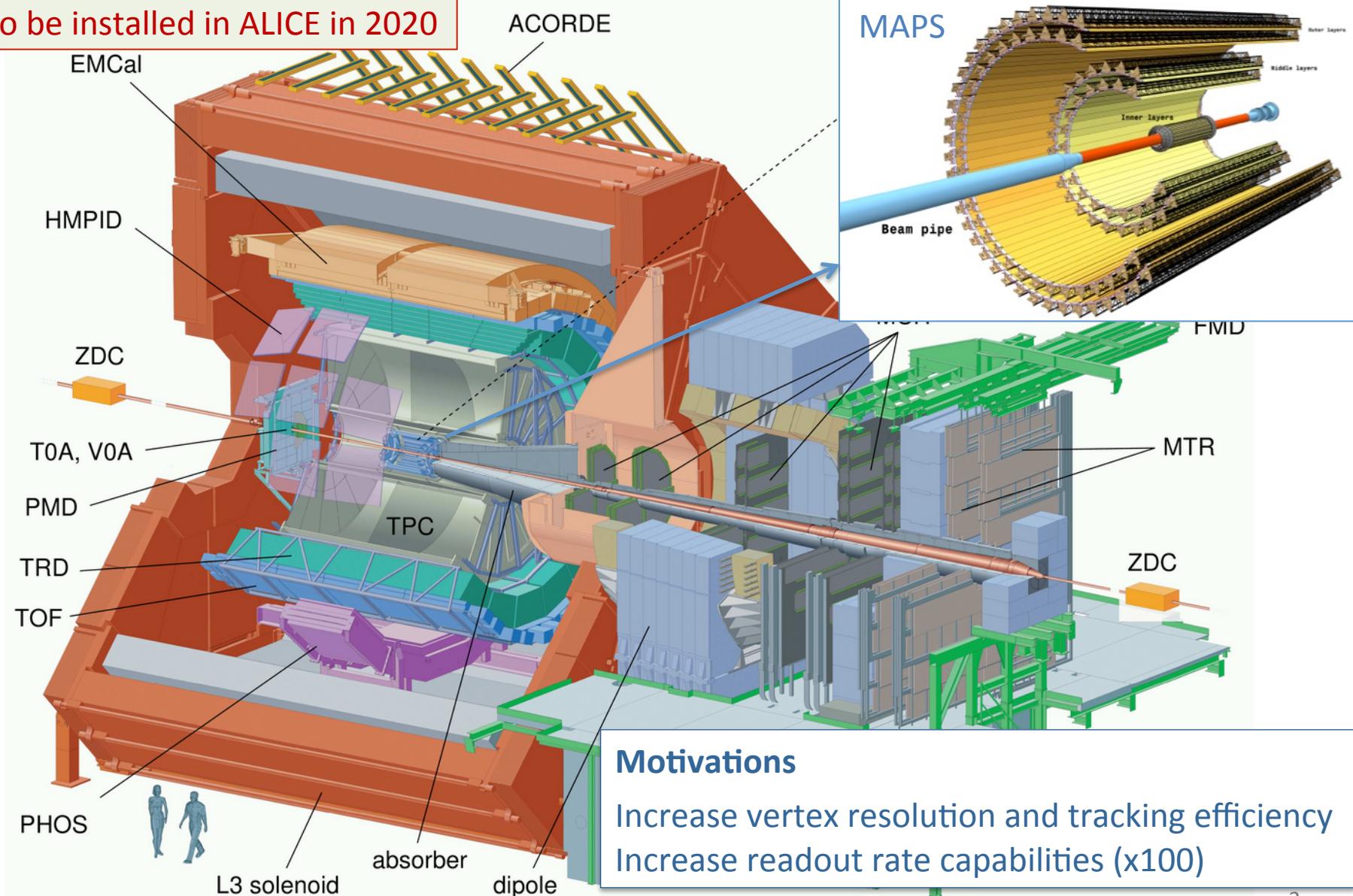
## OUTLINE

- ITS Upgrade: objectives, layout and performance
- Pixel Chip (sensor & readout)
- ITS upgrade main components
- Cost breakdown

# Upgrade of the ALICE Inner Tracking System



To be installed in ALICE in 2020



## Motivations

- Increase vertex resolution and tracking efficiency
- Increase readout rate capabilities (x100)

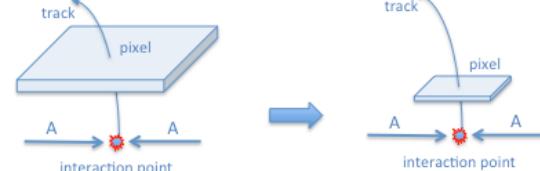
# ITS upgrade design objectives

A Large Ion Collider Experiment



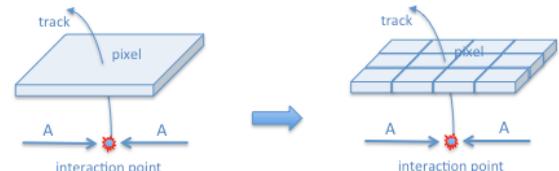
## 1. Improve impact parameter resolution by a factor of $\sim 3$

- Get closer to IP (position of first layer): 39mm  $\rightarrow$  23mm
- Reduce  $x/X_0$  /layer:  $\sim 1.14\%$   $\rightarrow \sim 0.3\%$  (for inner layers)
- Reduce pixel size: currently  $50\mu\text{m} \times 425\mu\text{m}$   $\rightarrow O(30\mu\text{m} \times 30\mu\text{m})$



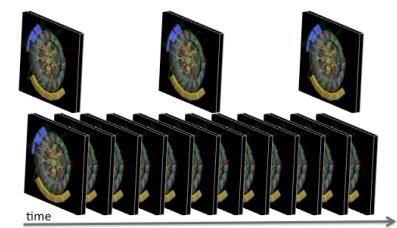
## 2. Improve tracking efficiency and $p_T$ resolution at low $p_T$

- Increase granularity:
  - 6 layers  $\rightarrow$  7 layers
  - silicon drift and strips  $\rightarrow$  pixels



## 3. Fast readout

- readout Pb-Pb interactions at  $> 100$  kHz  
(currently limited at 1kHz with full ITS)



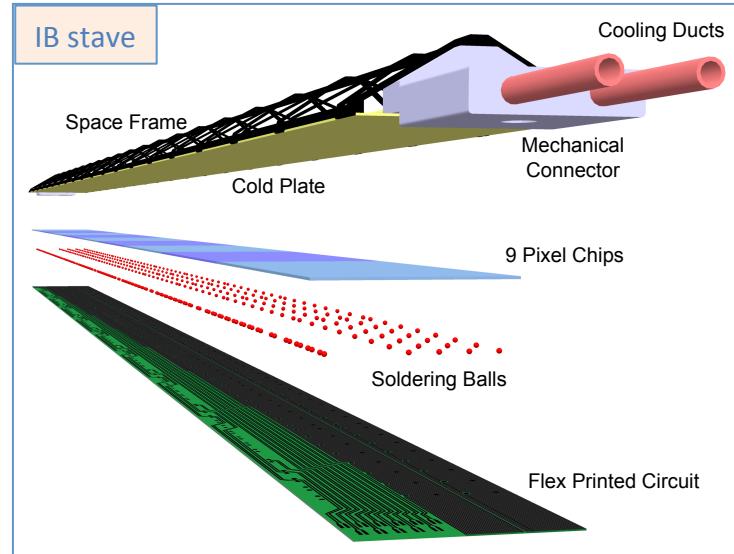
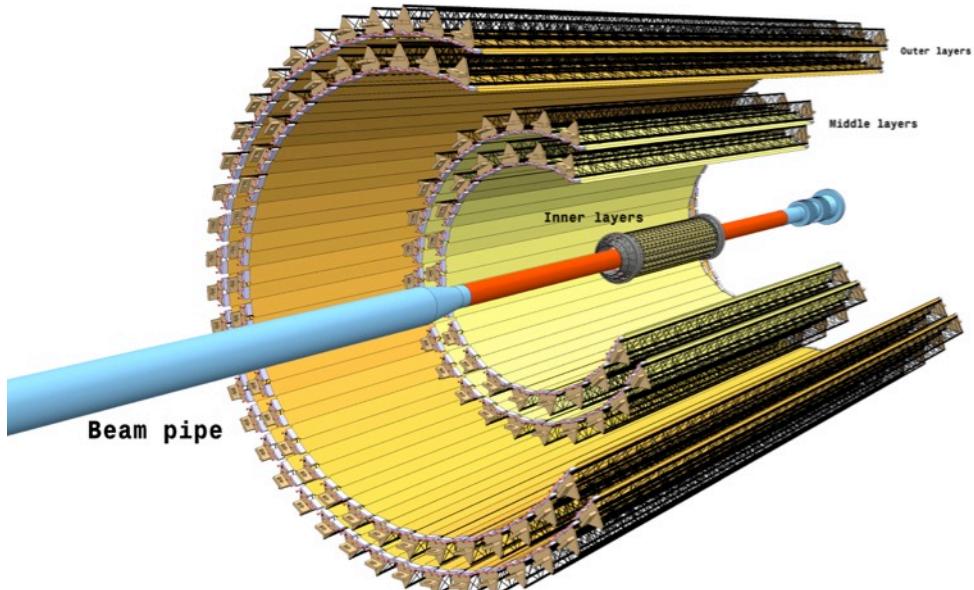
## 4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

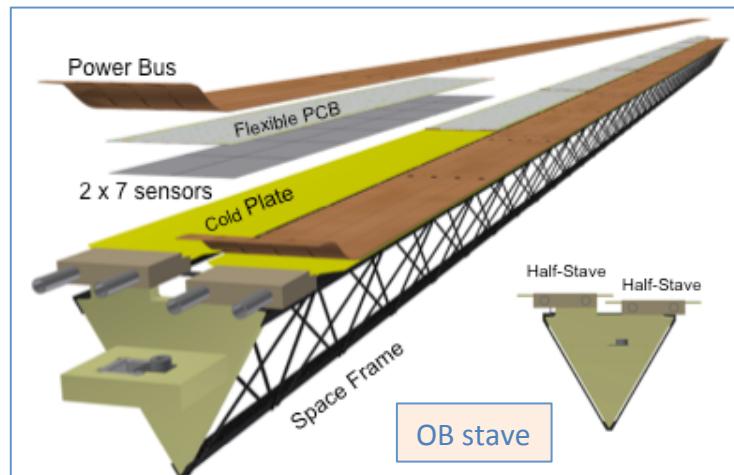
Install detector during LHCC LS2 (2019-20)

# New ITS Layout

A Large Ion Collider Experiment



- ▶ 7-layer barrel based on CMOS sensors
- ▶ Radial coverage 22 – 400 mm
- ▶ Total active area  $\sim 10\text{m}^2$
- ▶  $\sim 24,000$  pixel chips (12.5 G pixels)
- ▶ Radiation:  $\sim 2.7$  Mrad ( $\sim 1.7 \times 10^{13}$  1MeV  $n_{\text{eq}}/\text{cm}^2$ ) including safety factor 10

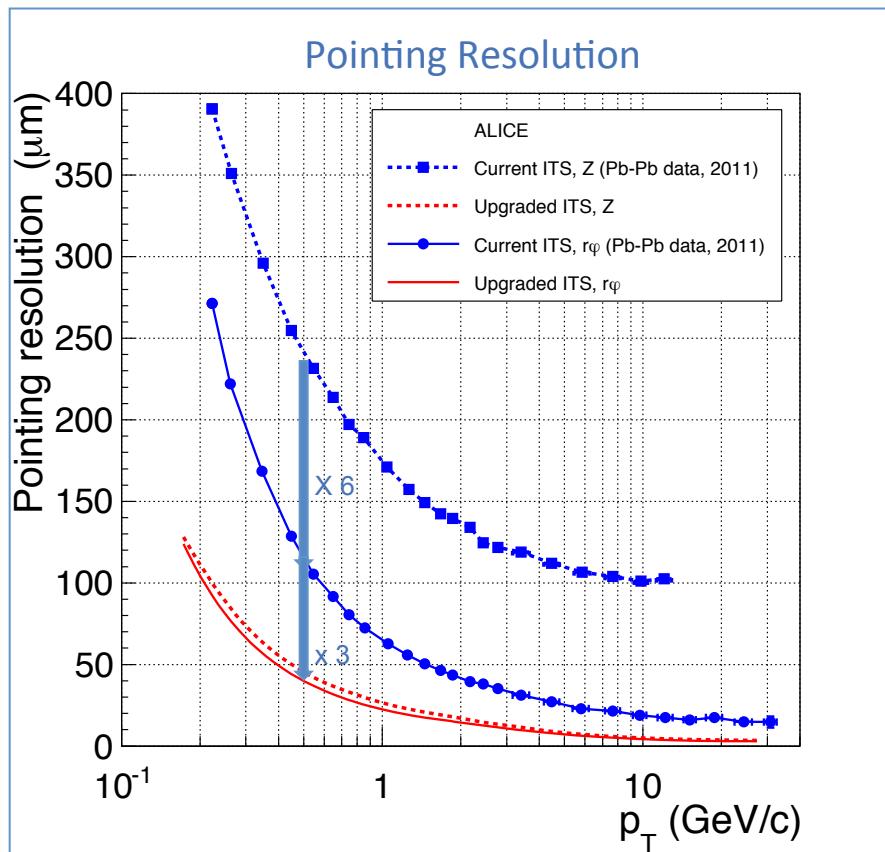


# Performance of new ITS (MC simulations)

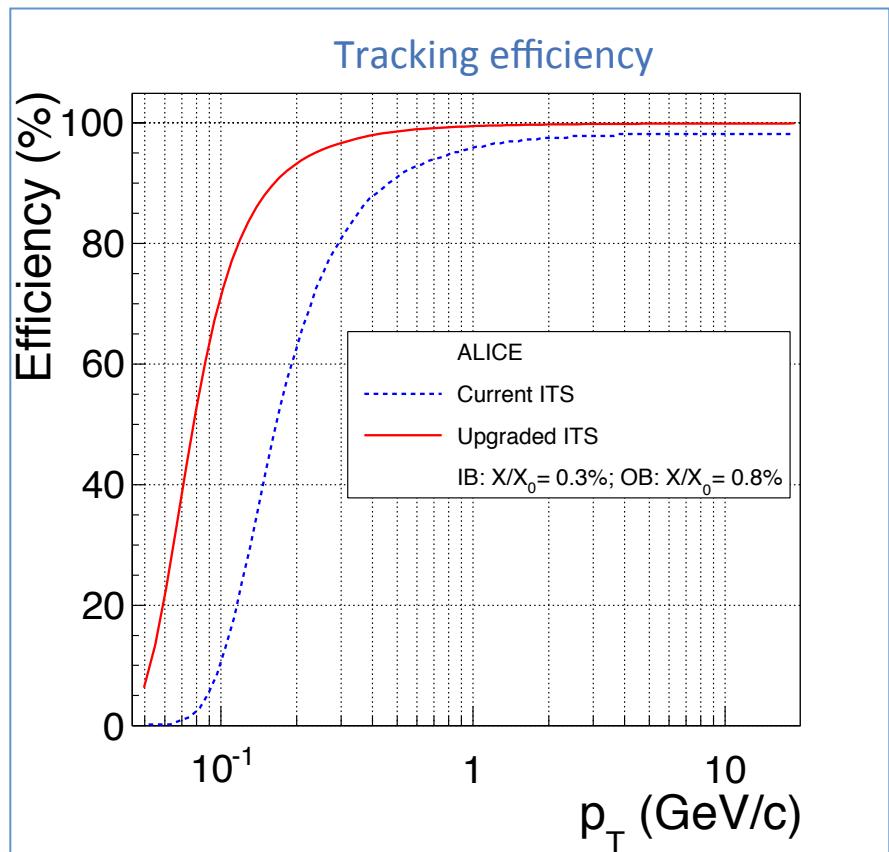
A Large Ion Collider Experiment



## Impact parameter resolution



## Tracking efficiency (ITS standalone)



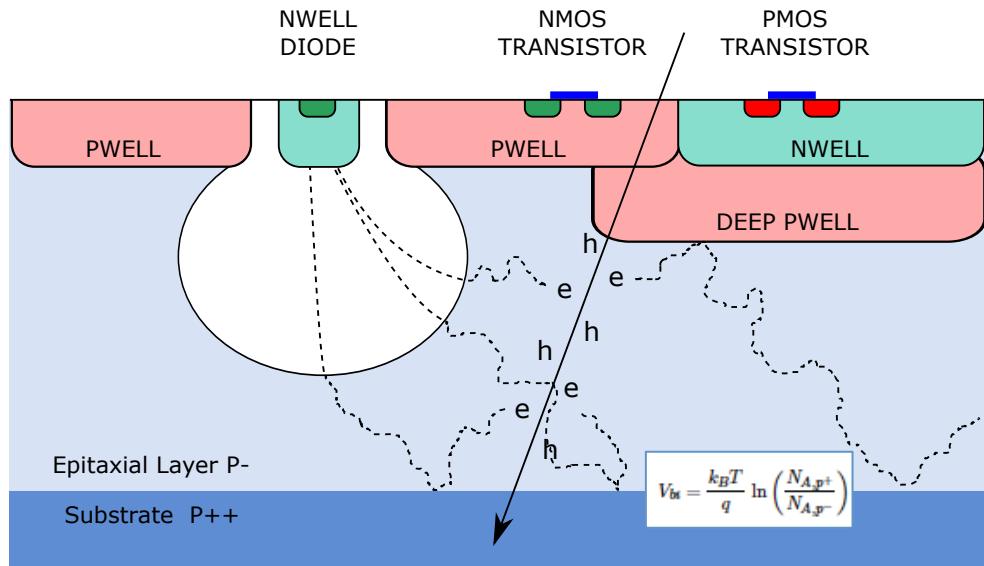
$\sim 40 \mu\text{m}$  at  $p_T = 500 \text{ MeV}/c$

# ITS Pixel Chip – technology choice

A Large Ion Collider Experiment



## CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



### Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

substrate:  $N_A \sim 10^{18}$

epitaxial layer:  $N_A \sim 10^{13}$

deep p-well:  $N_A \sim 10^{16}$

- ▶ High-resistivity ( $> 1\text{k}\Omega \text{ cm}$ ) p-type epitaxial layer (18-30  $\mu\text{m}$ ) on p-type substrate
- ▶ Small n-well diode (2  $\mu\text{m}$  diameter),  $\sim 100$  times smaller than pixel => low capacitance
- ▶ Application of (moderate) reverse bias voltage to substrate (contact from the top) can be used to increase depletion zone around NWELL collection diode
- ▶ Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry within active area

# PIXEL Chip – General Requirements

A Large Ion Collider Experiment

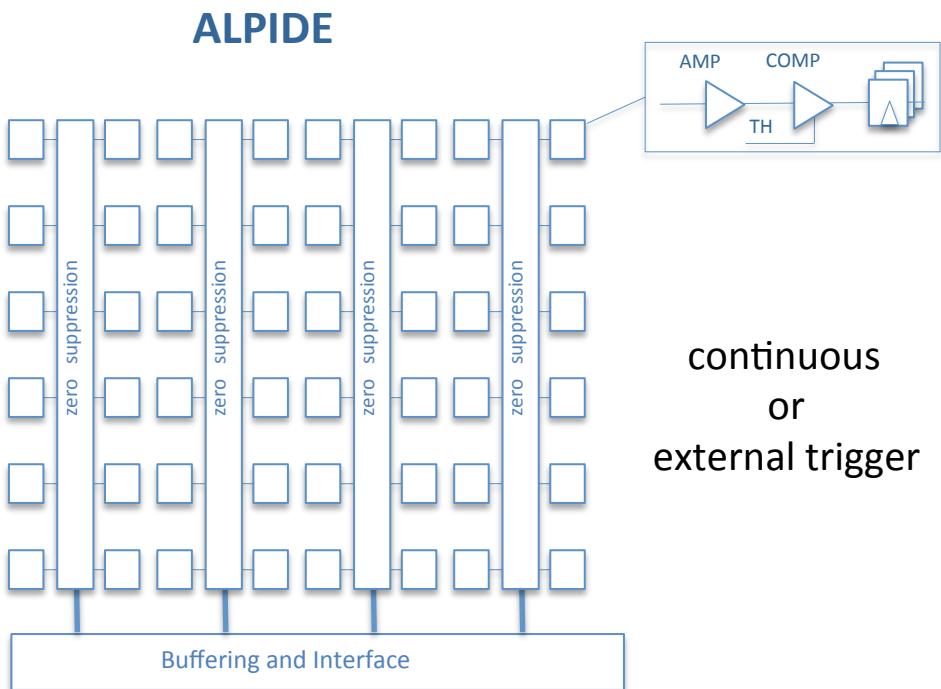


## General Requirements and ALPIDE Specifications<sup>(\*)</sup>

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)		<b>15 x 30</b>
Chip thickness ( $\mu\text{m}$ )	50	100
Spatial resolution ( $\mu\text{m}$ )	5	10 (5)
Detection efficiency		> 99%
Fake hit rate		$< 10^{-5} \text{ evt}^{-1} \text{ pixel}^{-1}$ (> ALPIDE)
Integration time ( $\mu\text{s}$ )		$< 30$ (< 10)
Power density (mW/cm <sup>2</sup> )	$< 300$ (~35)	$< 100$ (~20)
TID radiation hardness (krad) (*)	2700	100
NIEL radiation hardness (1MeV n <sub>eq</sub> /cm <sup>2</sup> ) (**)	$1.7 \times 10^{13}$	$1.7 \times 10^{12}$

(\*) Colour code: **ALPIDE specifications** if different from requirements

(\*\*) 10 x radiation load integrated over approved programme (~ 6 years of operation)



## Architecture

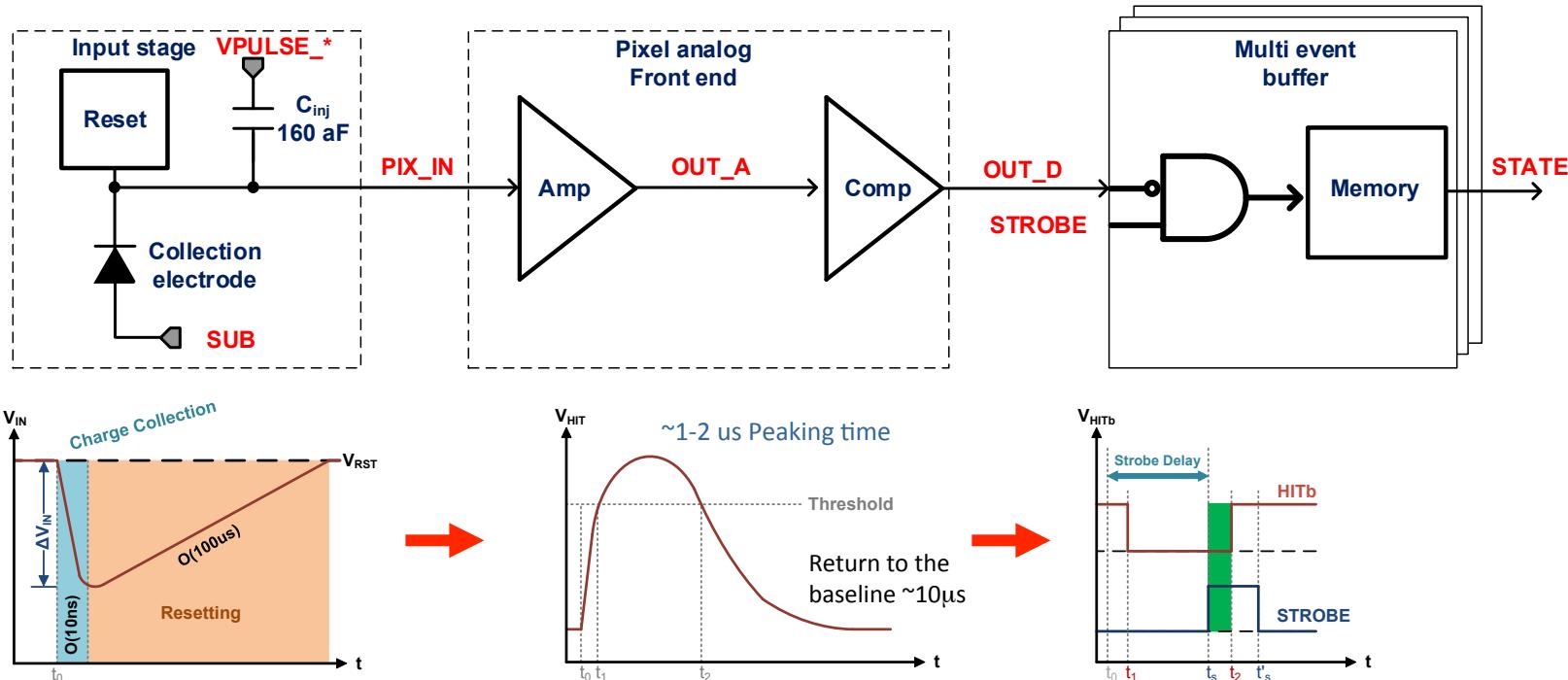
- ▶ In-pixel amplification
- ▶ In-pixel discrimination
- ▶ In-pixel (multi-) hit buffer
- ▶ In-matrix sparsification

## Key Features

- ◎ 28 µm x 28 mm pixel pitch
- ◎ Continuously active, ultra-low power front-end (**40nW/pixel**)
- ◎ No clock propagation to the matrix → ultra-low power matrix readout (**2mW whole chip**)
- ◎ Global shutter (<2µs): triggered acquisition or continuous

# ALPIDE Principle of Operation

A Large Ion Collider Experiment



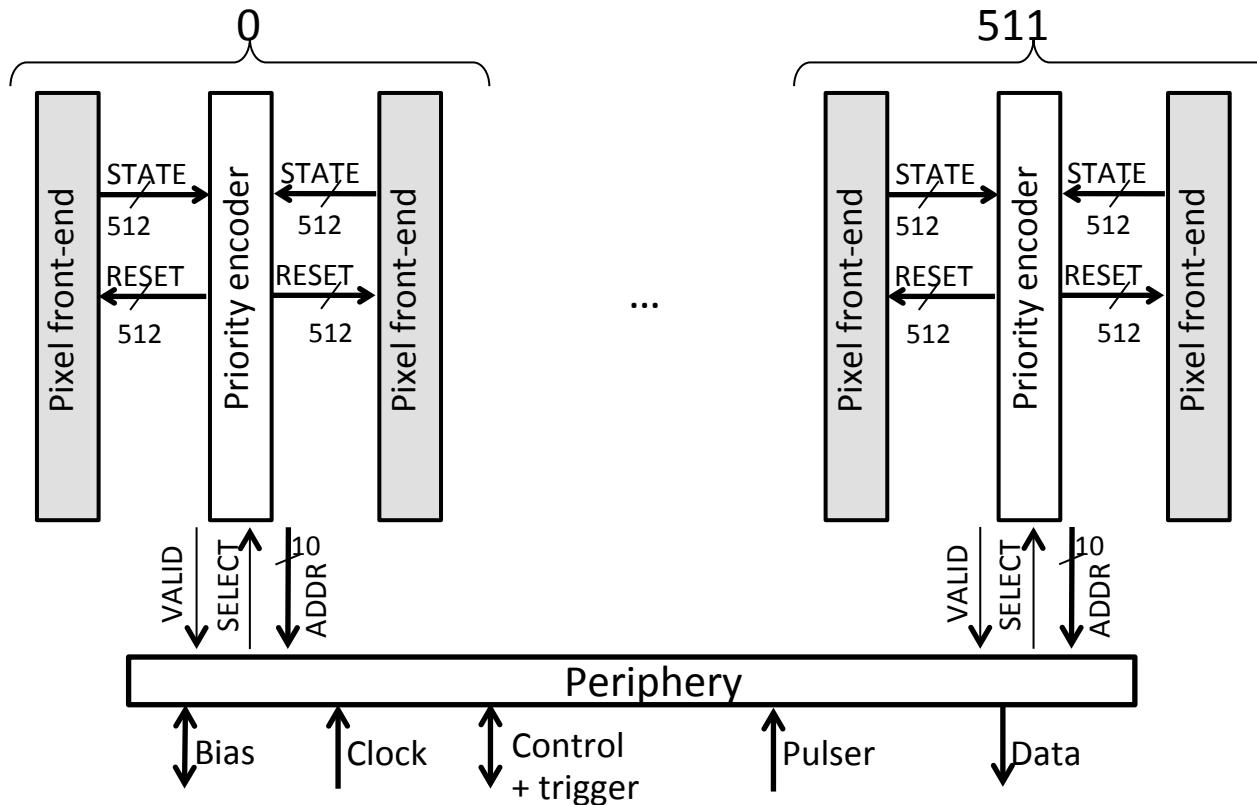
Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with  $\sim 1-2\mu\text{s}$  peaking time
- Threshold is applied to form binary pulse
- Hit is latched into a (3-bit) memory if strobe is applied during binary pulse

ultra low-power front-end circuit  
40nW / pixel

# ALPIDE Principle of Operation

A Large Ion Collider Experiment



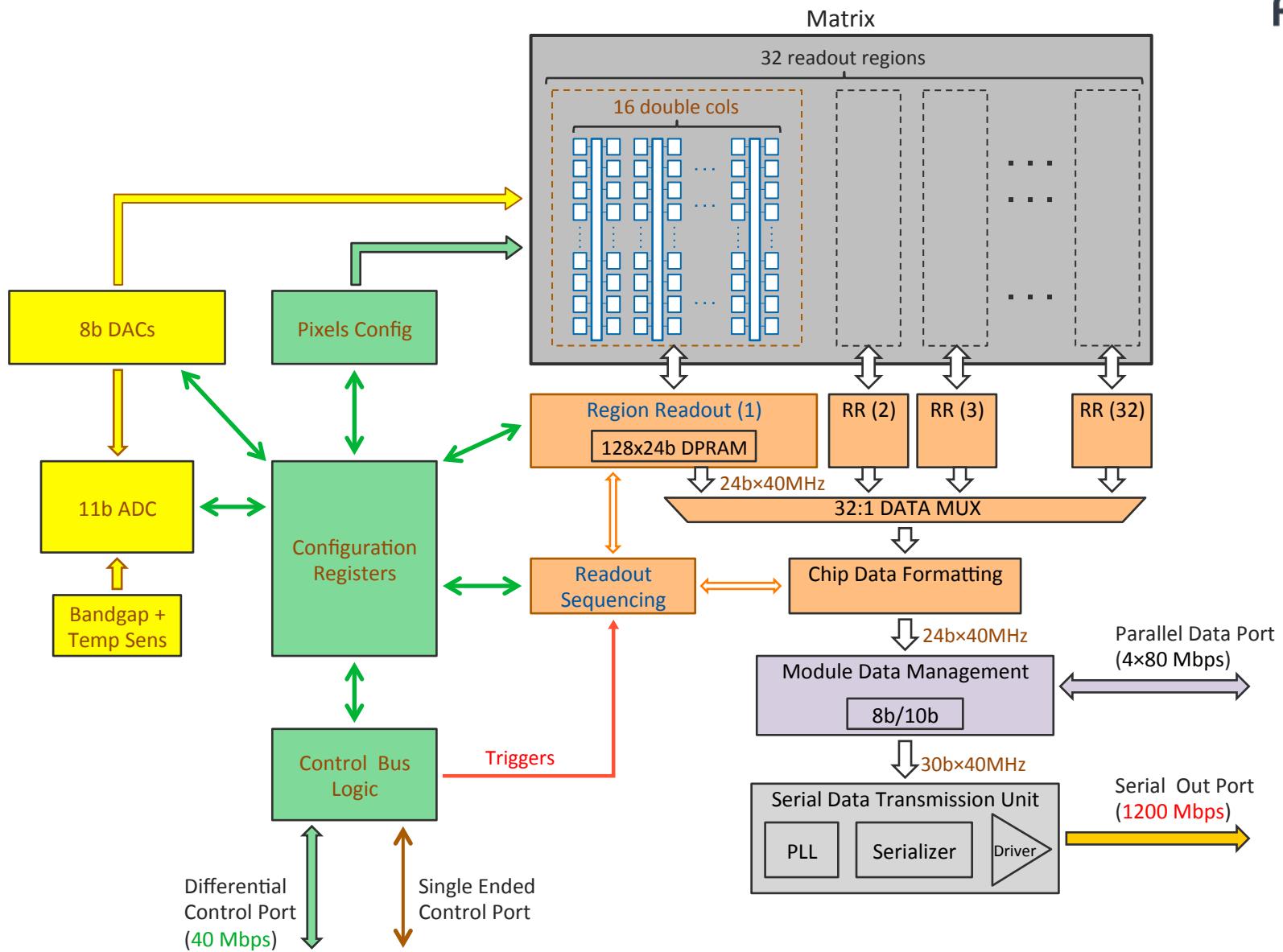
Pixel Matrix - Hit driven architecture

low-power matrix readout  $\sim 2\text{mW}$

- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit (**no free running clock**)  $\rightarrow$  low power

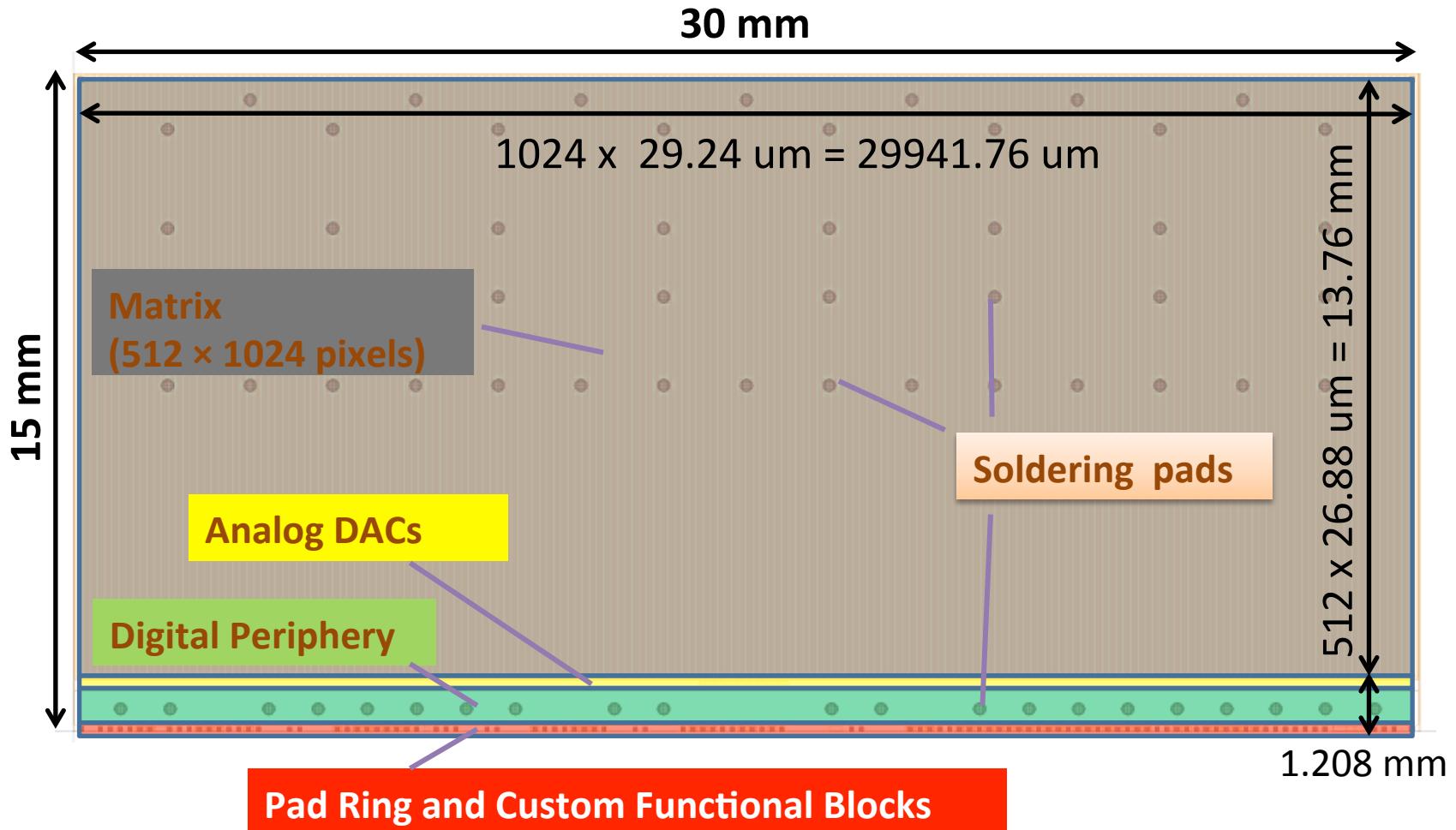
# ALPIDE Readout Control Features

A Large Ion Collider Experiment



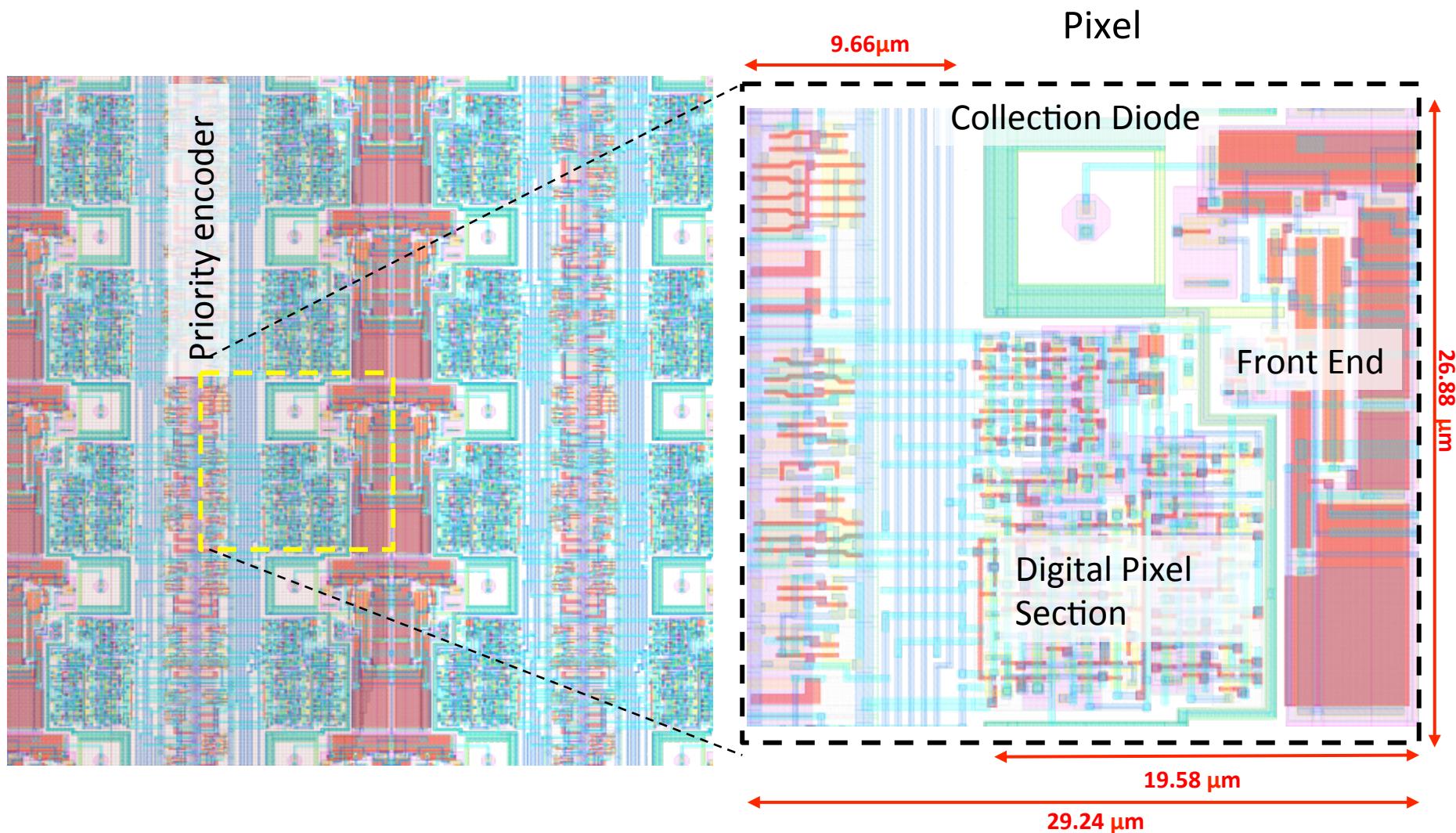
# ALPIDE Chip Floorplan

A Large Ion Collider Experiment



# Matrix Layout

A Large Ion Collider Experiment



# Periphery Layout

A Large Ion Collider Experiment



Pixels and Priority Encoders

Analog DACs

Digital Periphery

Pad Ring

Soldering pad

Memory Macros

Sea of gates

Regular pads + Custom blocks

1.208 mm

0.120 mm

1.1 mm

0.220 mm

# ALPIDE Development

A Large Ion Collider Experiment



# pALPIDE3 – Main Design Features

A Large Ion Collider Experiment



ALPIDE full-scale prototypes v1 (2014), v2 (May 2015)

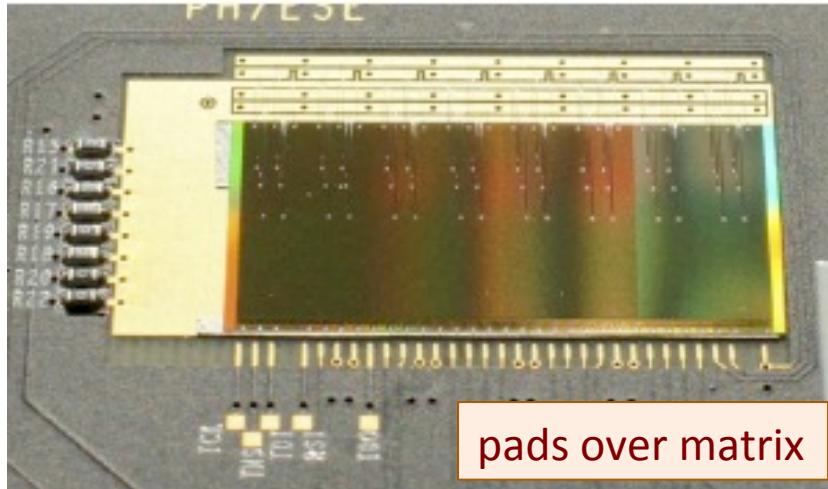
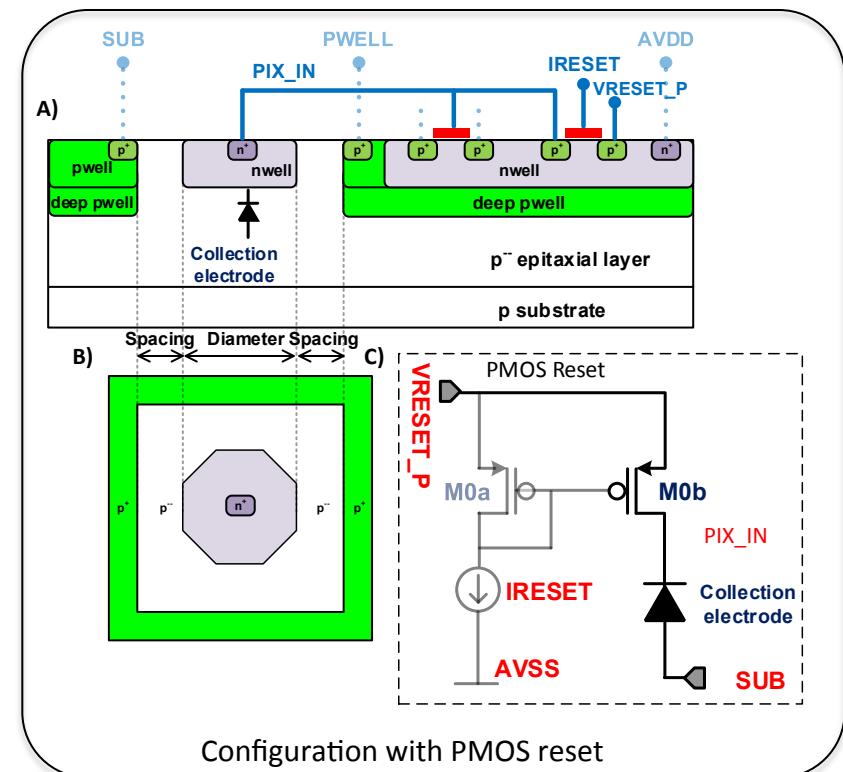


Figure: picture of pALPIDE-2

## pALPIDE-3 main parameters

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28 $\mu$ m x 28 $\mu$ m
- Integration time: <10 $\mu$ s
- Power consumption: < 40mW/cm<sup>2</sup>
- 4 sectors with different pixels

Matrix divided in 4 sectors, each with 128 cols x 512 rows  
Collection node: octagonal shape 2 $\mu$ m diameter  
Spacing between NWELL and PWELL: 2 $\mu$ m - 4 $\mu$ m  
2 reset mechanism: diode, PMOS

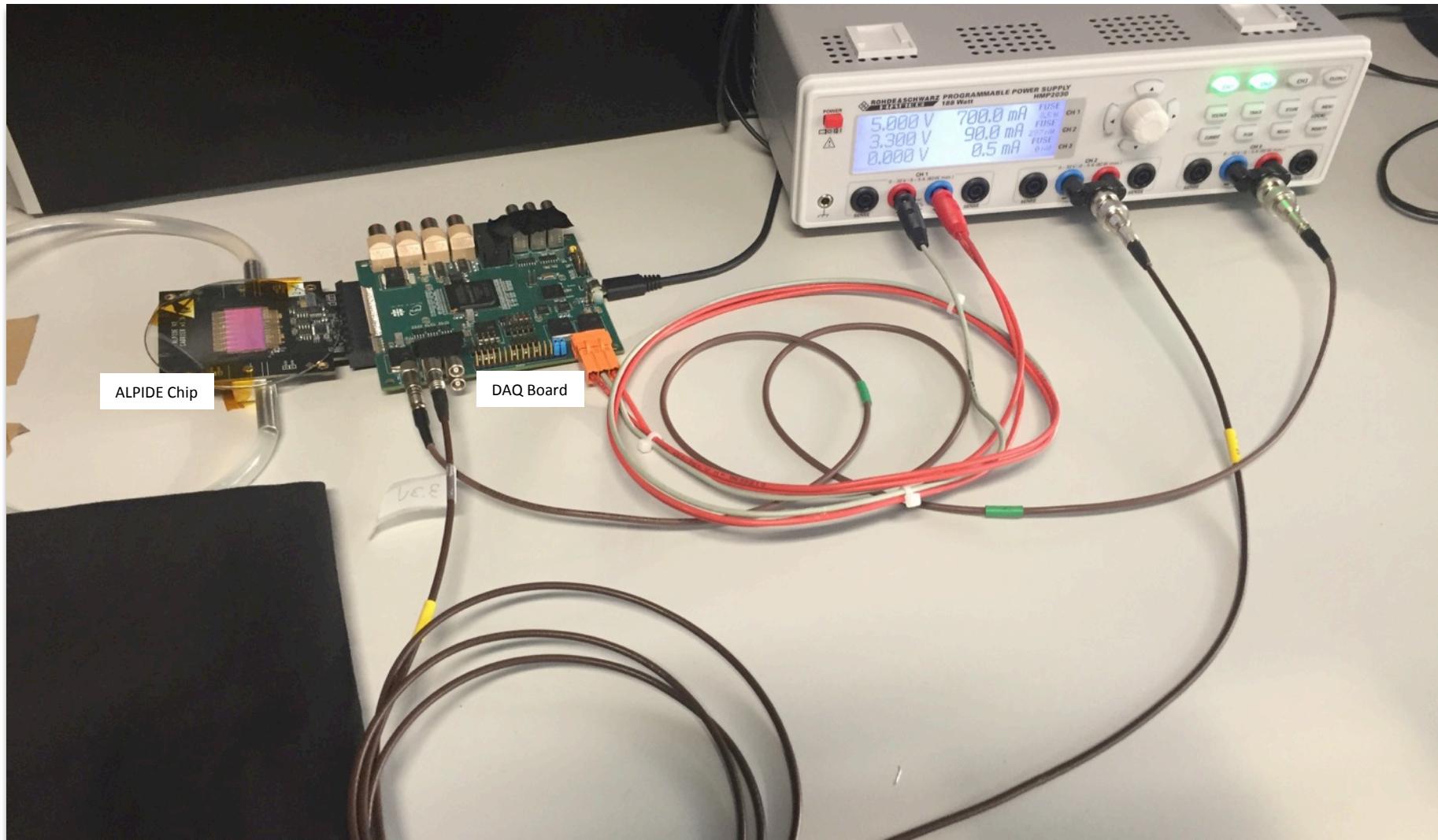


# Experimental Results

A Large Ion Collider Experiment



Laboratory Measurements → e.g. noise and thresholds

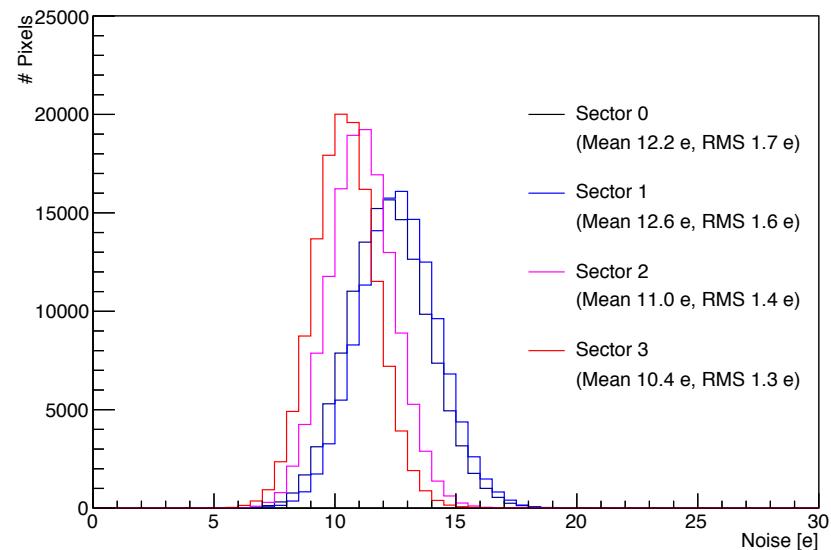
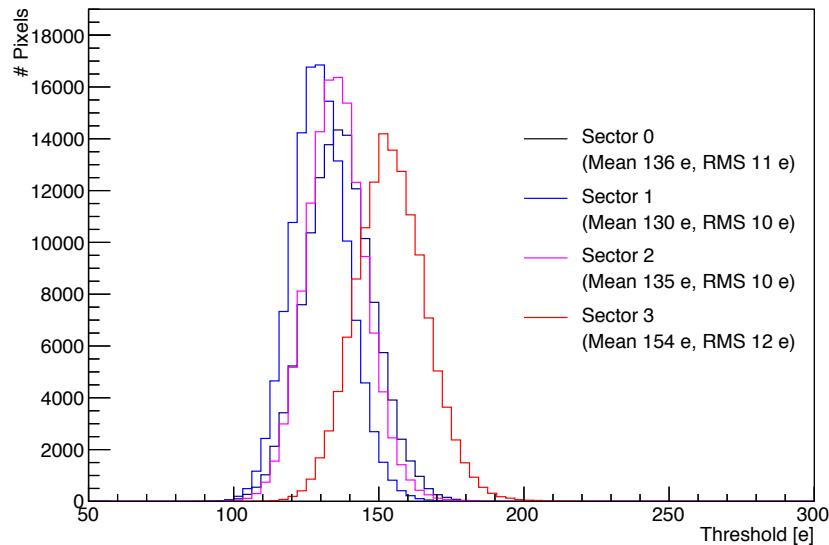


# Experimental Results – pALPIDE-2

A Large Ion Collider Experiment



## Example of Threshold and Noise Distributions



$$V_{\text{SUB}} = -3V, I_{\text{THR}} = 0.5\text{nA}, V_{\text{CASN}} = 0.95V$$

- ▶ All sectors behave qualitatively similarly
- ▶ Noise is about the same value as threshold RMS
- ▶ Threshold about 10 x higher than noise
- ▶ Threshold 7 x smaller than most-probable energy loss signal of a MIP in 18 μm of silicon

# Experimental Results – pALPIDE-2

A Large Ion Collider Experiment



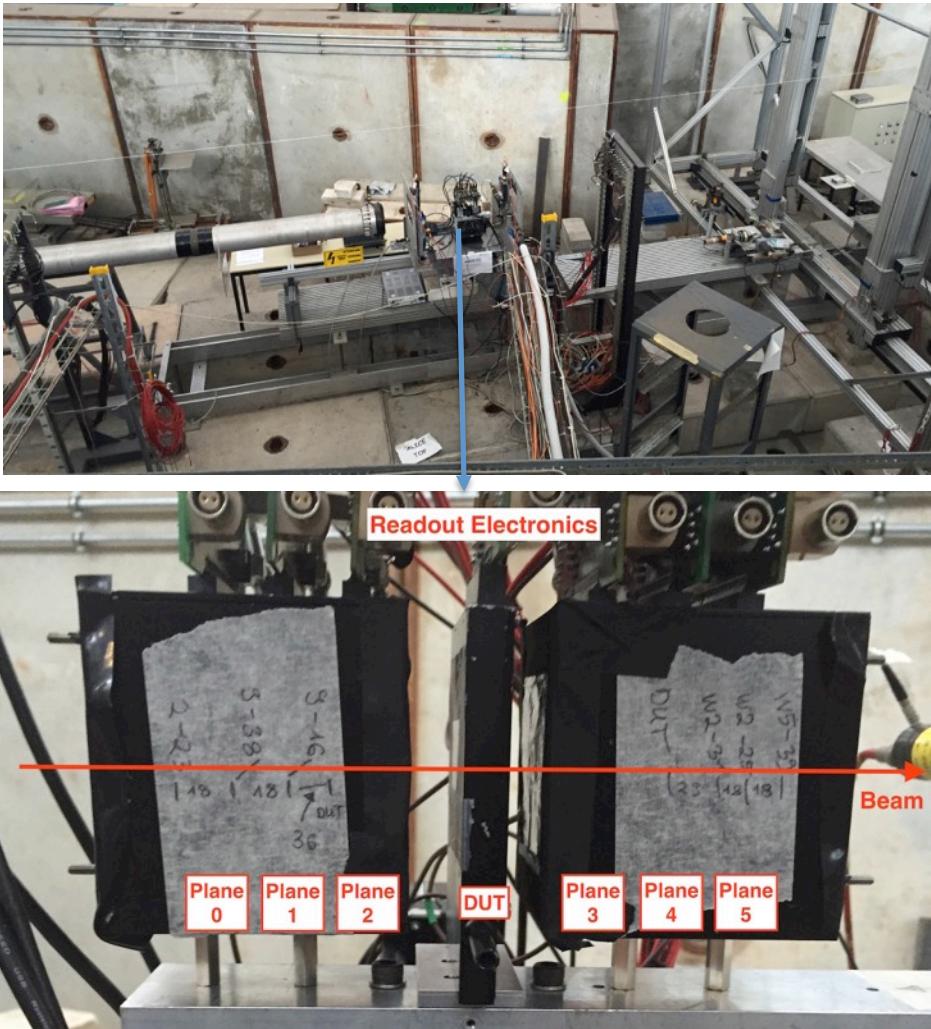
Characterization at several test beam facilities: CERN, Pohang, SLRI, Frascati

## Test Beam Set-up

- ▶ 6 GeV/c  $\pi^-$  beam at CERN PS
- ▶ 6 reference planes based on pALPIDE-1
- ▶ Single pALPIDE-2 as Device Under Test (DUT) in the center
- ▶ Track resolution of about  $2.8\mu\text{m}$  ( $< 28\mu\text{m}$ )

## Analysis Method

- ▶ Extrapolate track from reference planes through DUT
- ▶ Search for clusters next to extrapolated impinging point → **detection efficiency**
- ▶ Obtain **cluster size**
- ▶ Compare extrapolated and actual position → **position resolution**



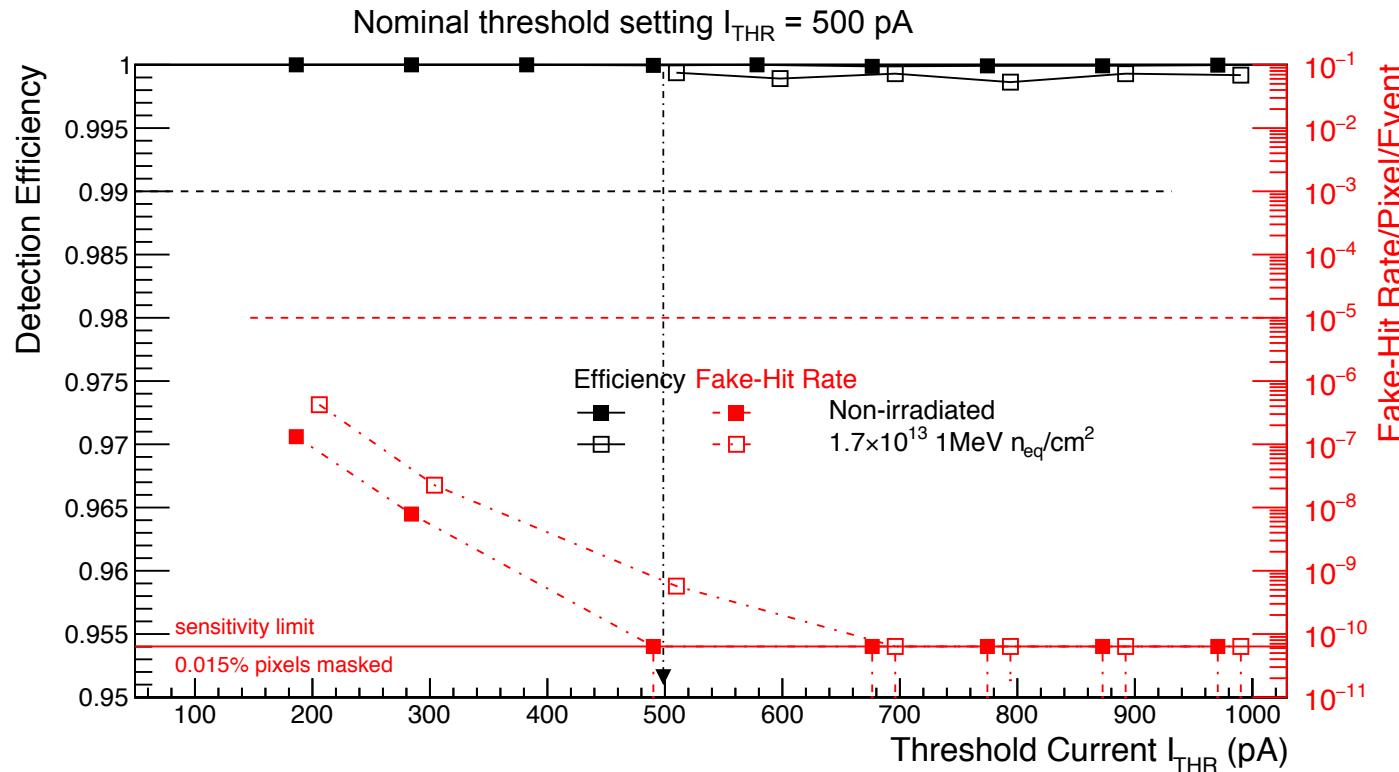
# Experimental Results – pAlpide-2

A Large Ion Collider Experiment



## Efficiency and fake hit rate

epi=30 $\mu$ m, V<sub>BB</sub>=-6V, spacing=4 $\mu$ m



Even larger operation margin for 30 $\mu$ m epi layer and 4 $\mu$ m spacing

- Results refer to chips with 30 $\mu$ m high-res epi layer, thinned to 50  $\mu$ m:  
1 non irradiated and 1 irradiated with  $10^{13}$  1MeV  $n_{eq} / cm^2$

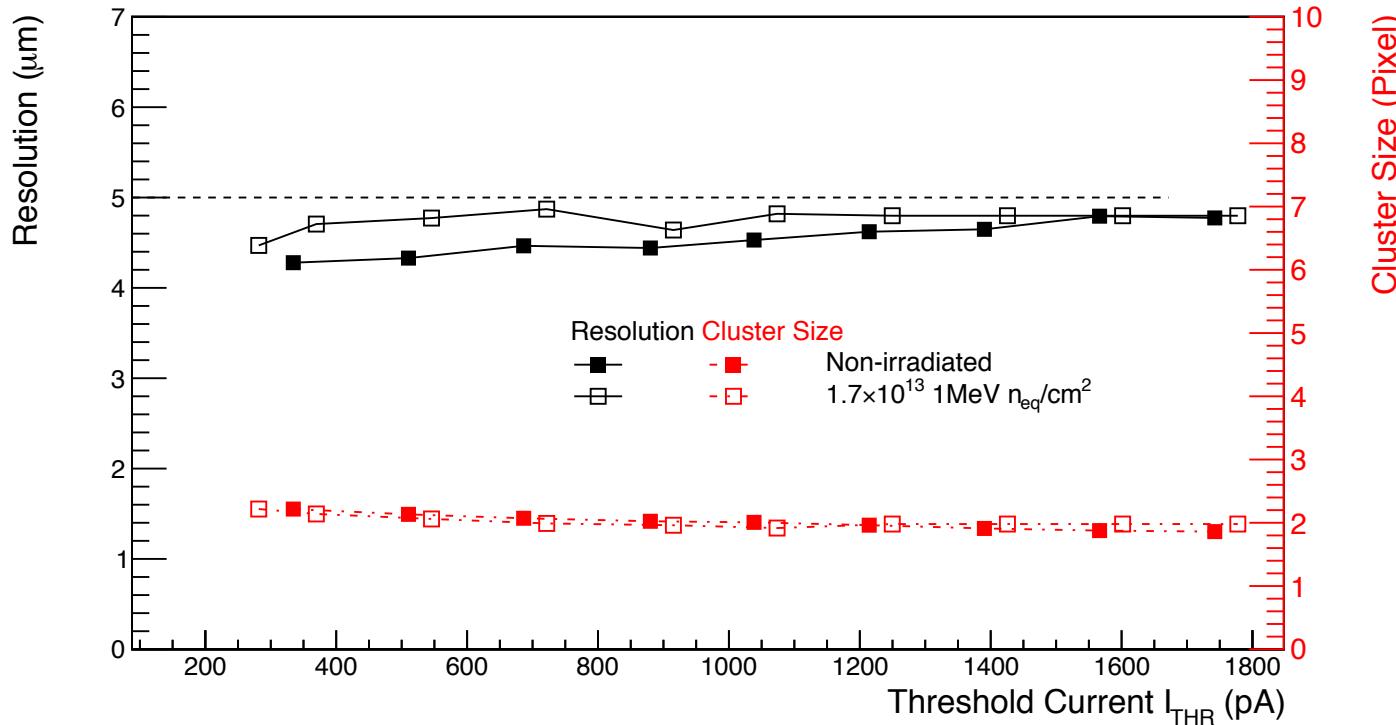
# Experimental Results – pAlpide-2

A Large Ion Collider Experiment



## Spatial Resolution and Cluster Size

epi=30 $\mu$ m, V<sub>BB</sub>=-6V, spacing=4 $\mu$ m



$\sigma_{det} \approx 5 \mu\text{m}$  is achieved before and after irradiation

- Results refer to chips with 30 $\mu$ m high-res epi layer, thinned to 50  $\mu$ m  
1 non irradiated and 1 irradiated with  $1.7 \times 10^{13} \text{ 1MeV } n_{eq} / \text{cm}^2$

# Experimental Results – pALPIDE-3

A Large Ion Collider Experiment

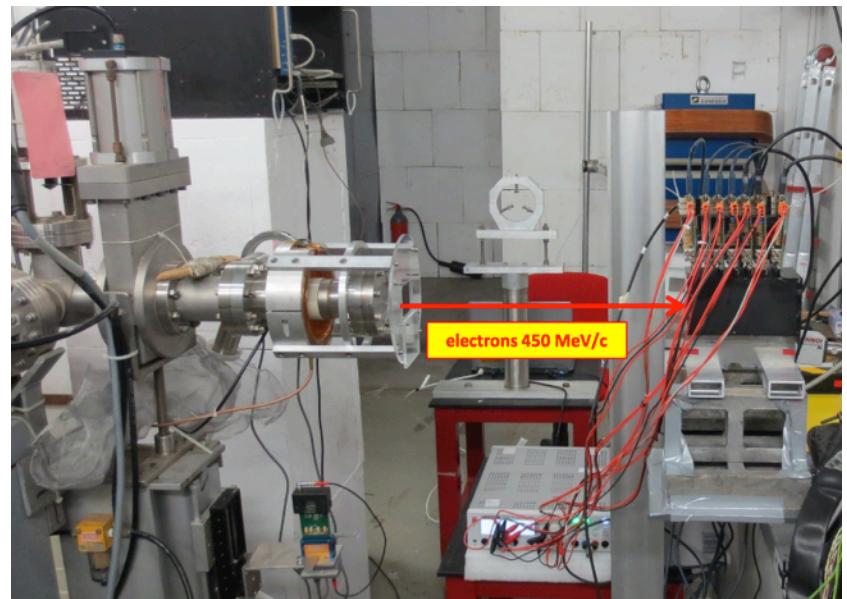
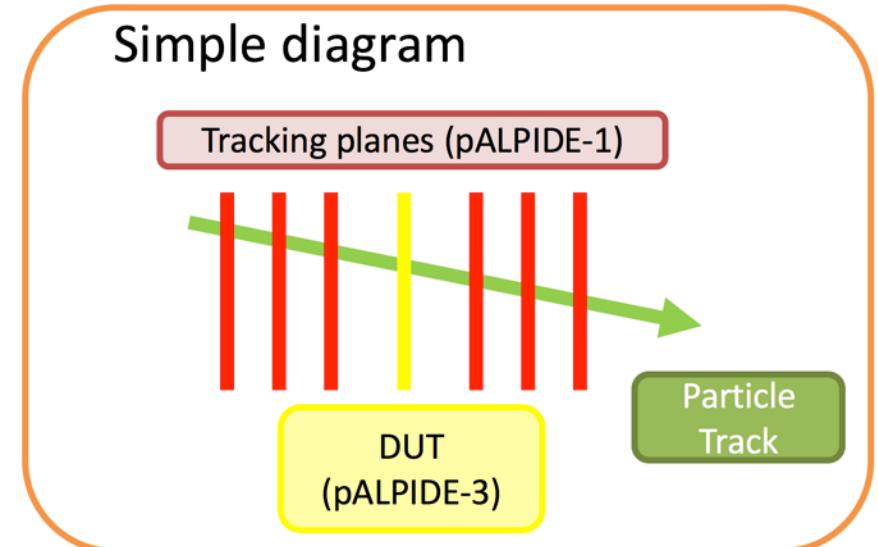


## Test Beam Set-up

- ▶ 450 MeV/c  $e^-$  beam at Frascati (BTF)
- ▶ 6 reference planes based on pALPIDE-1
- ▶ Single pALPIDE-3 as Device Under Test (DUT) in the center

## Analysis Method

- ▶ Extrapolate track from reference planes through DUT
- ▶ Search for clusters next to extrapolated impinging point → **detection efficiency**
- ▶ Obtain **cluster size**



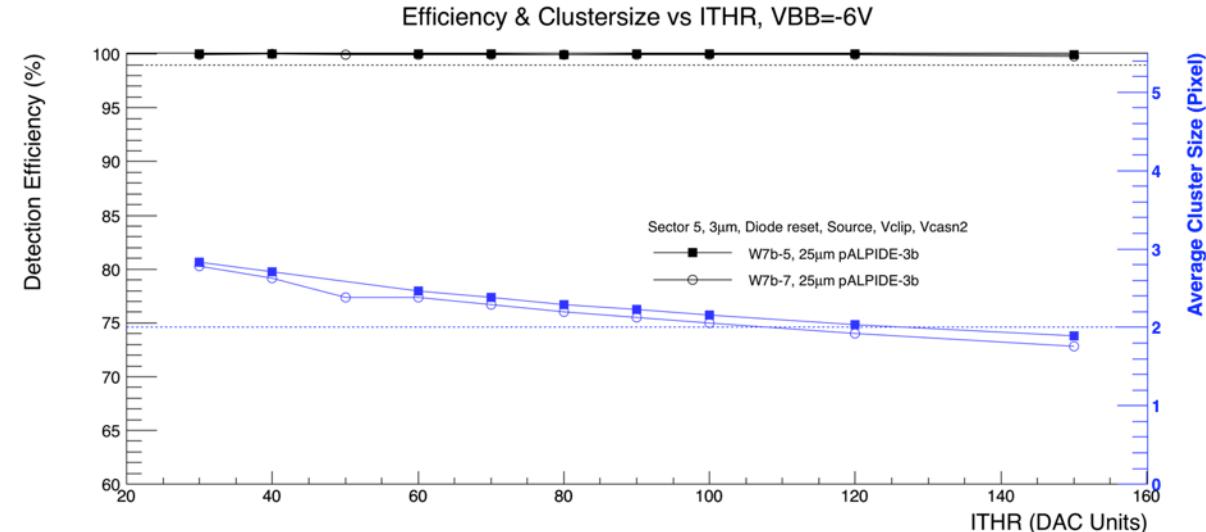
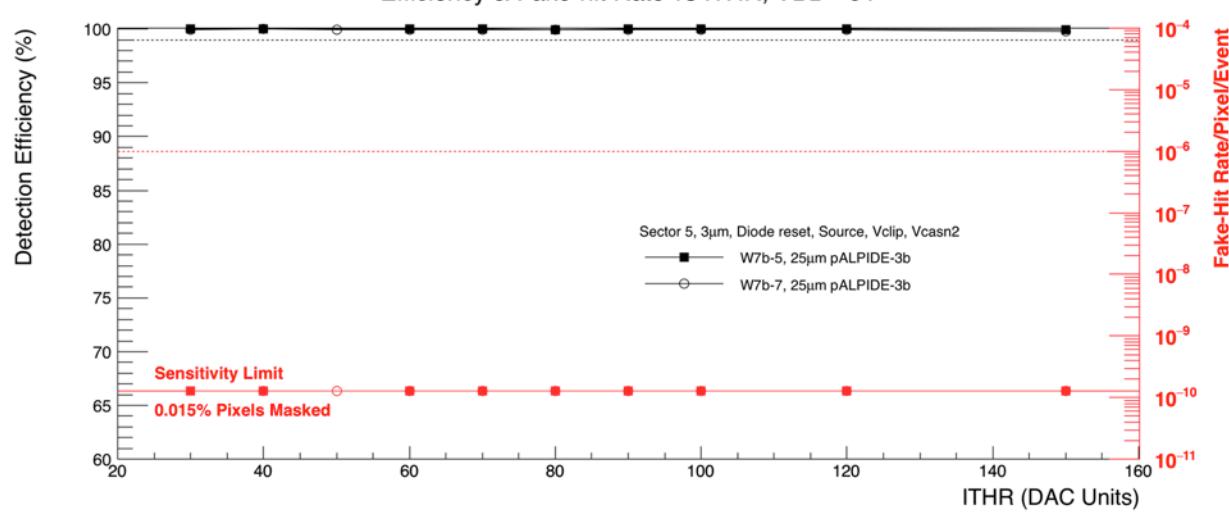
# Experimental Results – pAlpide-3

A Large Ion Collider Experiment



## Efficiency, fake hit rate, cluster size

$e\pi=25\mu\text{m}$ ,  $V_{BB}=-6\text{V}$ , spacing=3 $\mu\text{m}$

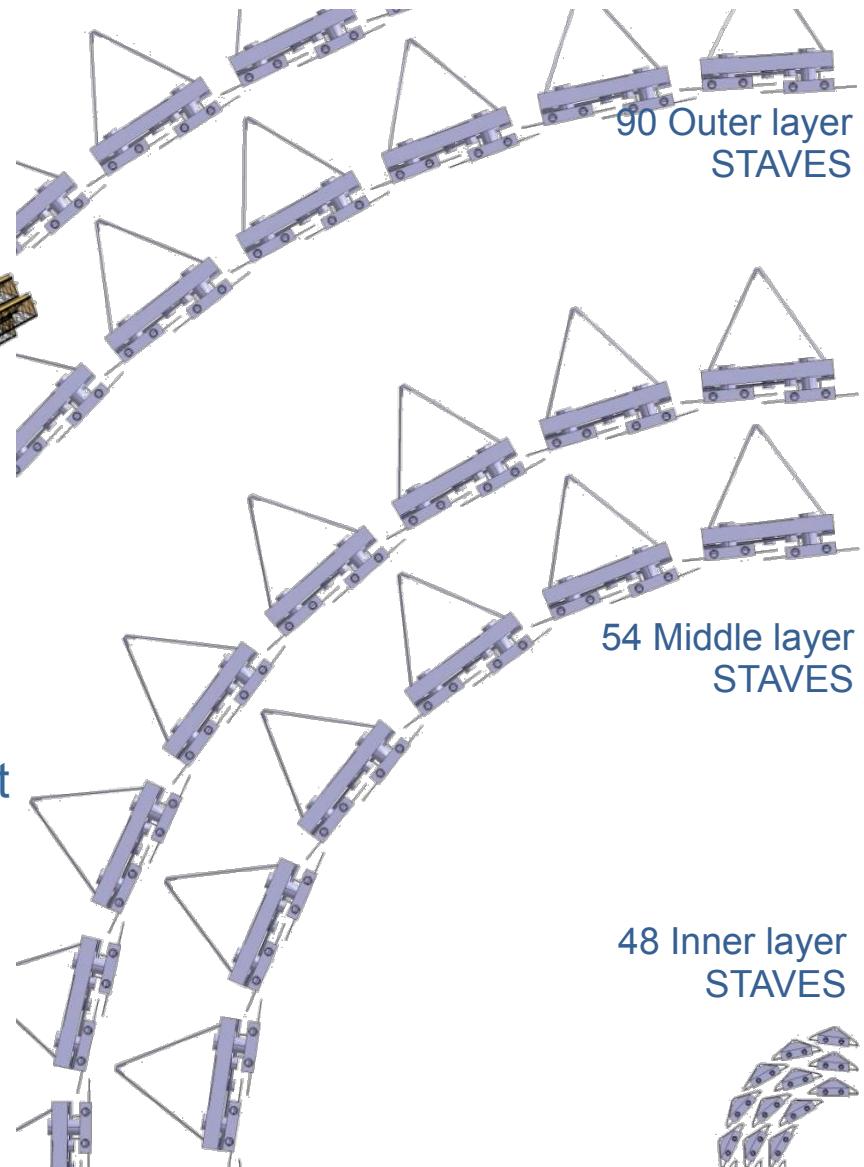
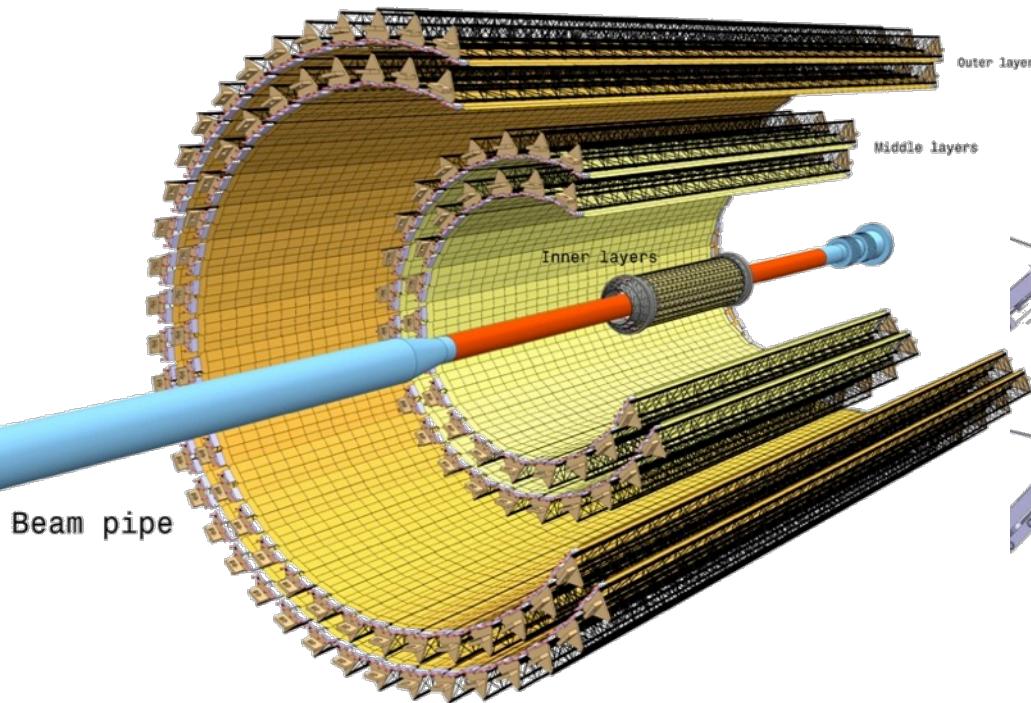


# New ITS layout

A Large Ion Collider Experiment



ALICE



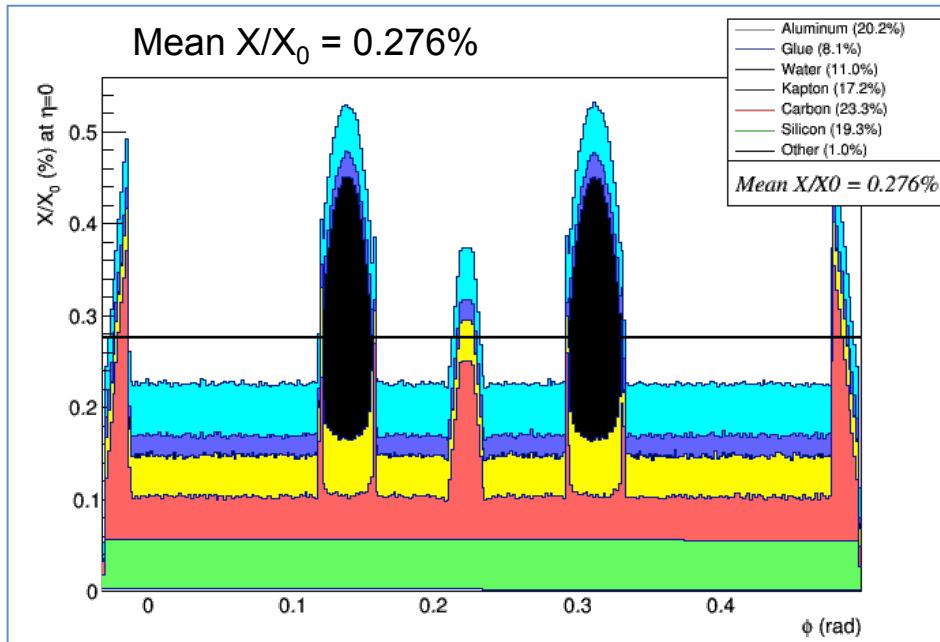
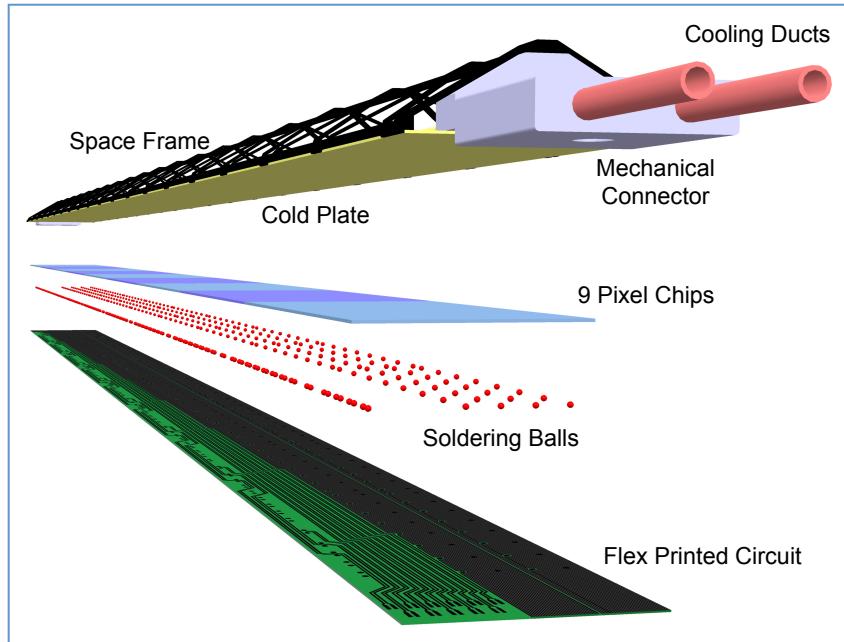
ITS layers are (azimuthally) segmented in staves, which are mechanically independent

## Staves length

Inner Layers	290mm
Middle Layers	900mm
Outer Layers	1500mm

# New ITS Layout - Inner Barrel Stave

A Large Ion Collider Experiment



$\langle \text{Radius} \rangle$  (mm): 23, 31, 39

Nr. of staves: 12, 16, 20

Nr. of chips/layer: 108, 144, 180

Power density: < 40 mW/cm<sup>2</sup>

Length in z (mm): 290

Nr. of chips/stave: 9

Material thickness:  $\sim 0.3\% X_0$

Throughput (@100kHz):  $\sim 80 \text{ Mb/s} \times \text{cm}^{-2}$

# Interconnection of Pixel Chip to Flex PCB

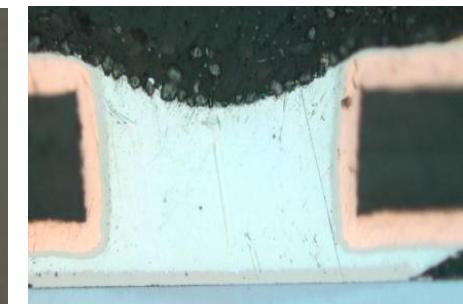
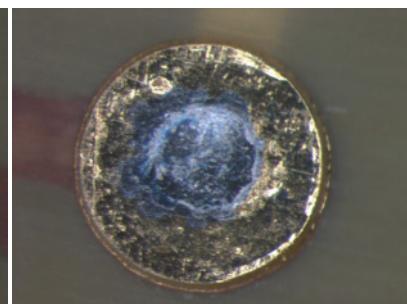
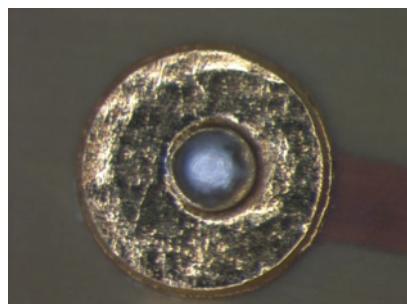
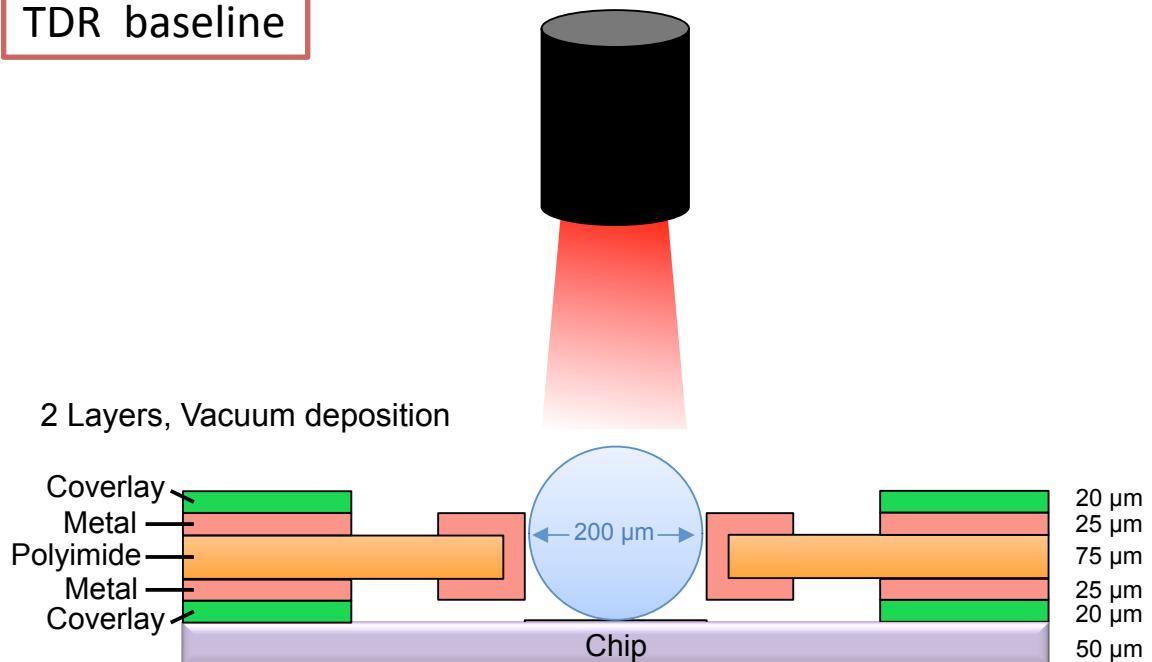
A Large Ion Collider Experiment



## Selective Laser Soldering



TDR baseline



# Interconnection of Pixel Chip to Flex PCB

A Large Ion Collider Experiment



## Selective Laser Soldering

All main issues were solved

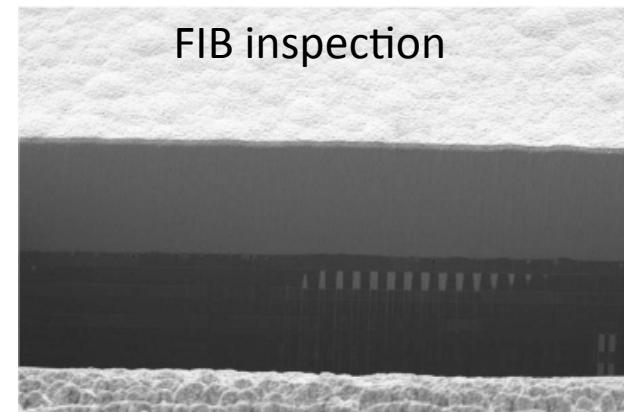
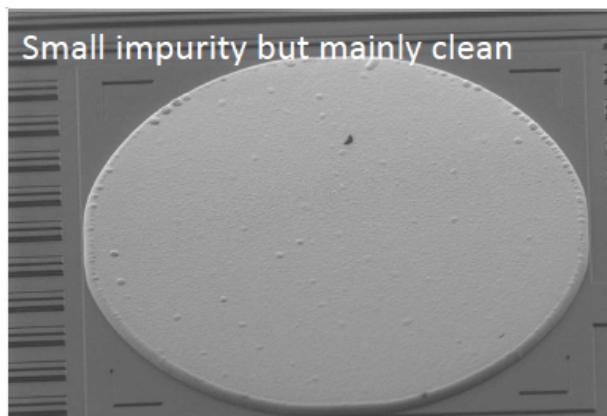
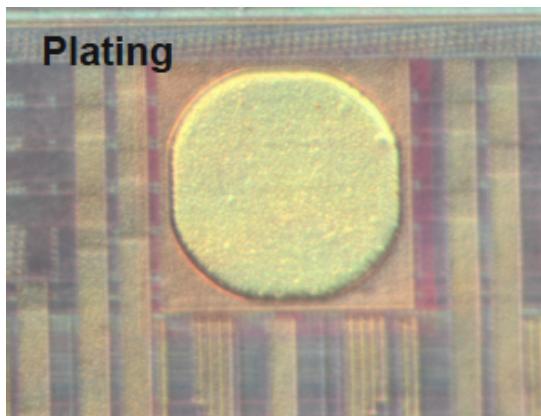
- Quality of the metallization of FPC VIAs
- Excessive warping of pixel chip
- Assembly jigs out of tolerance



Nevertheless the yield continued to be unsatisfactory

=> too often “cold” soldering or partial wetting of the pad

We investigated in detail (optical inspections, SEM, FIB and EDS analysis) the quality of the metallization of the interface pads, but everything seems according to specs

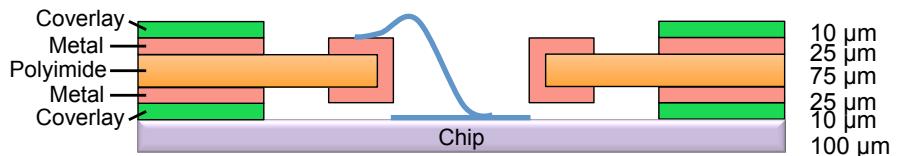


# Interconnection of pixel chip to flex PCB

A Large Ion Collider Experiment

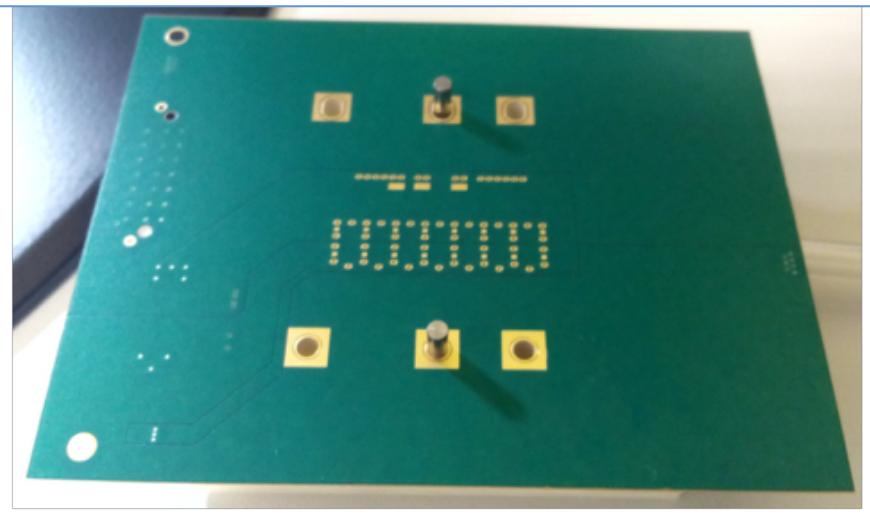


## Wire bonding

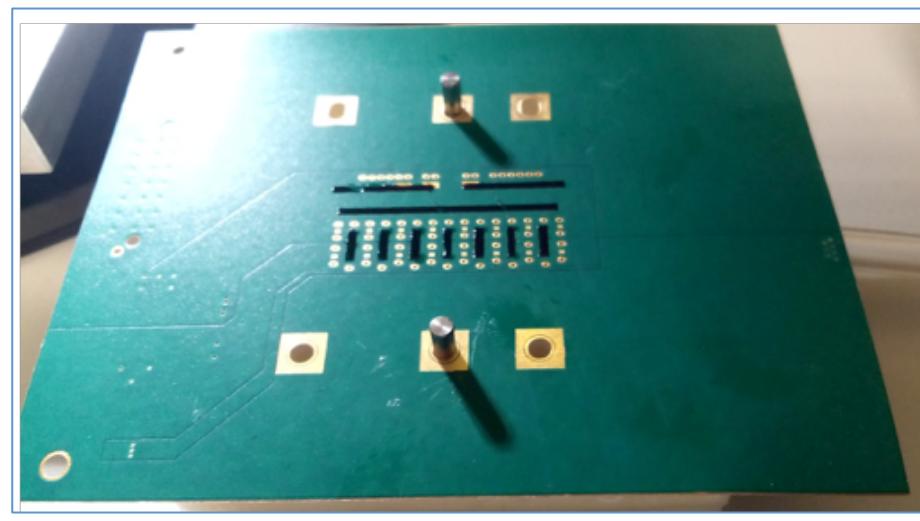


- The chip is glued on the electrical substrate (FPC)
- Electrical interconnection to the FPC using standard wedge (Al) wire bonding through the FPC VIAs

First tests done in January with single-chip assemblies



Flexible Printed Circuit (FPC)



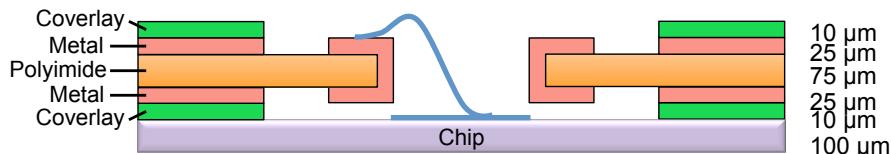
Glue dispensing (ECCOBOND45)

# Interconnection of pixel chip to flex PCB

A Large Ion Collider Experiment



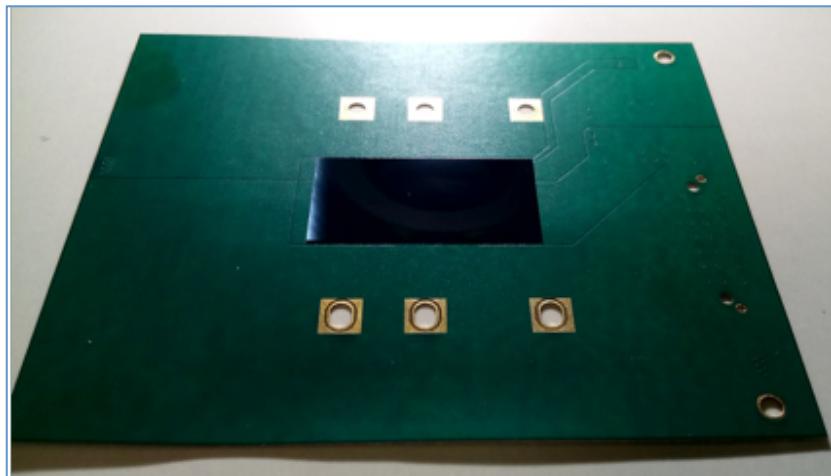
## Wire bonding



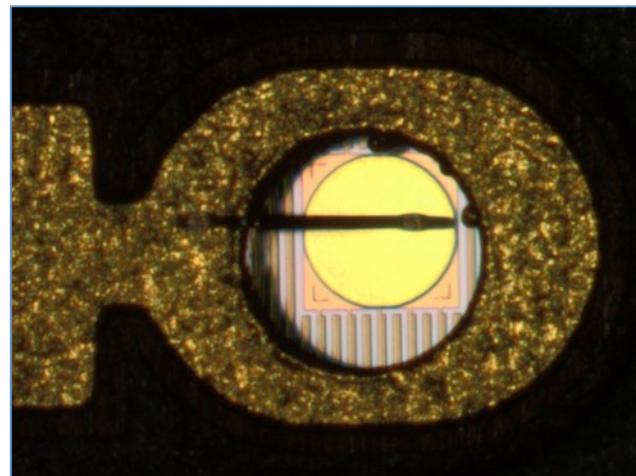
### Tests with pALPIDE-3 single-chip HIC

- 5 with 25μm Al wire and standard wedge tool
- 1 with 25μm Al wire and deep access wedge tool
- **Results: all working according to specs**

First tests done in January with single-chip assemblies



Chip glued on the FPC



Wire Bonding

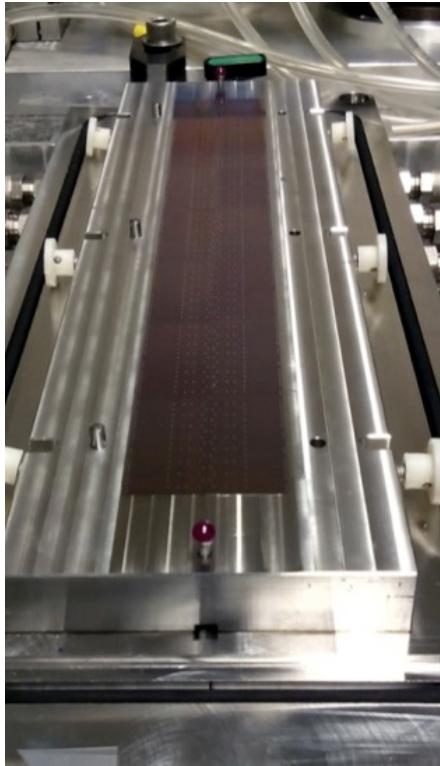
# Interconnection of pixel chip to flex PCB

A Large Ion Collider Experiment

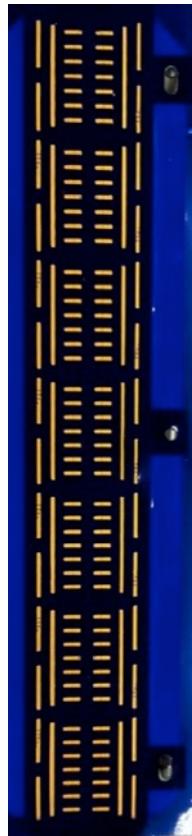


## Wire bonding – Outer Barrel HIC

Several IB and OB HICs were successfully assembled and characterized



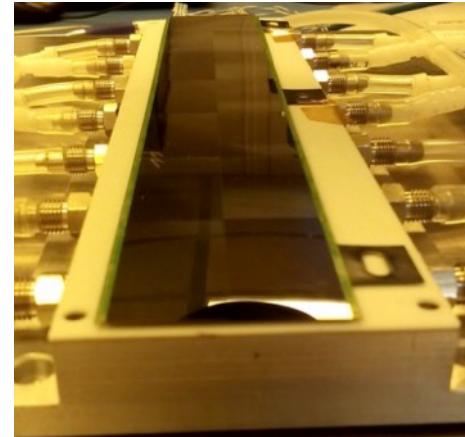
Alignment of chips



FPC with 80  $\mu\text{m}$  thick adhesive mask



Glue dispensed over the FPC after  
the removal of the mask



Top and Bottom view of the glued assembly

# Interconnection of pixel chip to flex PCB

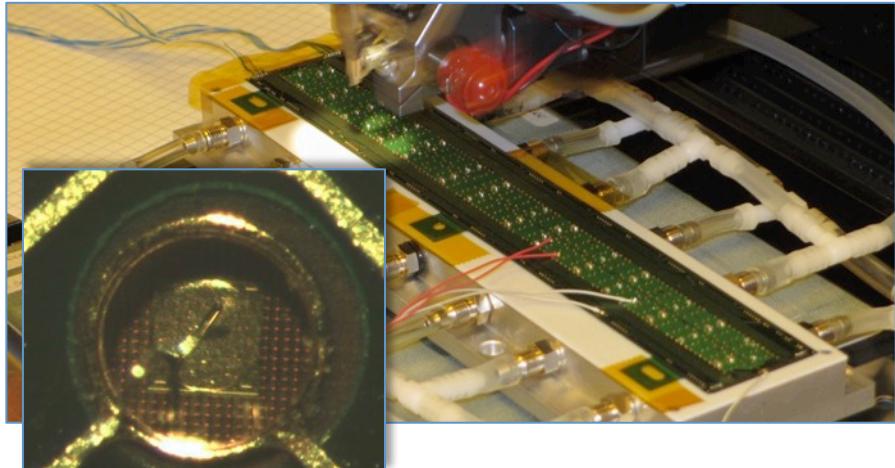
A Large Ion Collider Experiment



## Wire bonding – Outer Barrel HIC

HIC for the Outer Barrel is being assembled with its 14 pALPIDE-3 chips

Wire bonding



### Test of first HIC

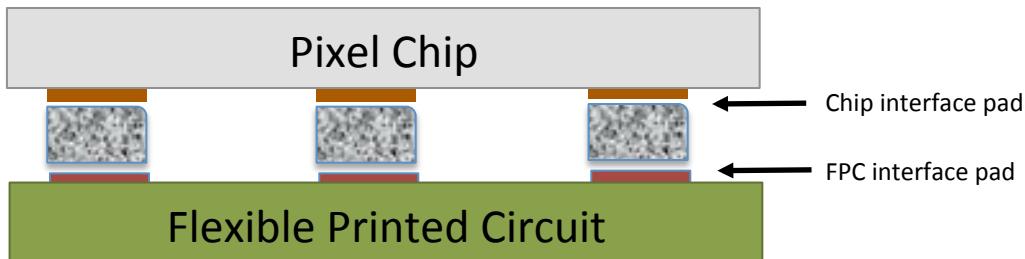
- First results (three HICs) show nominal behavior according to specs

# Interconnection of pixel chip to flex PCB

A Large Ion Collider Experiment



## Isotropic Conductive Adhesive



## Two types of conductive adhesives

- ABLESTIK 57C (curing at room temperature)
- AREMKO 556 LV (curing at room temperature)

## Interface pad

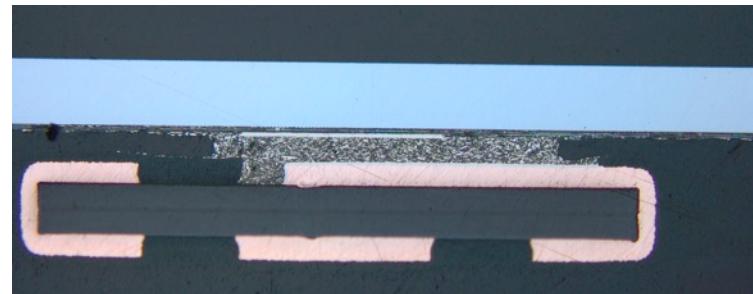
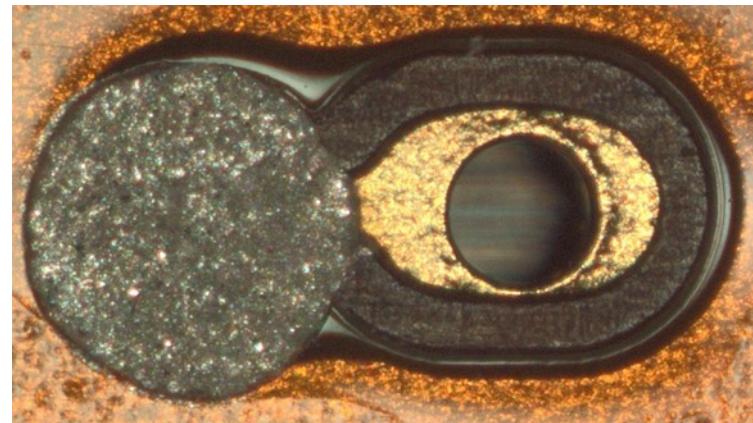
- Ni-Au plating

## Glue dispensing

- screen printing directly on FPC  
interface pad surface using a stencil

## Conductive Adhesives Under study

- Matrix: epoxy resin
- Filler: silver particles
- Polymerization at room T

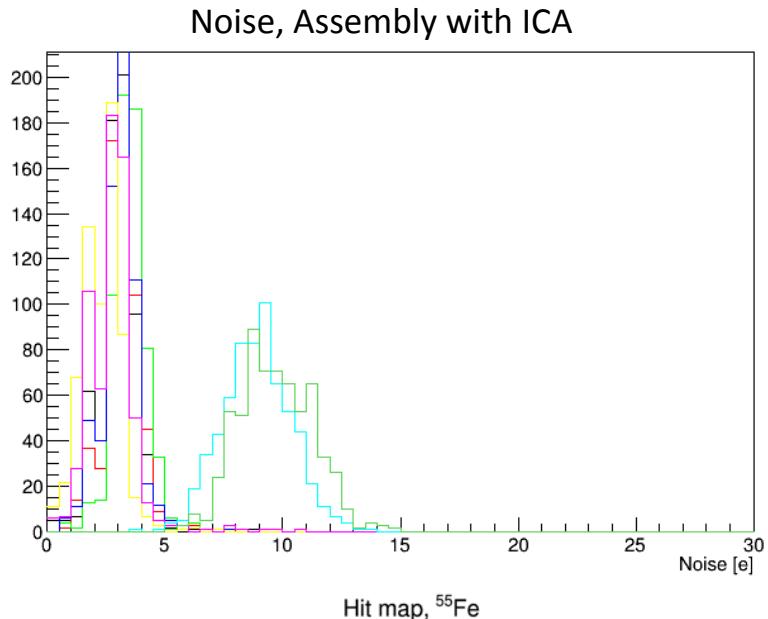


# Interconnection of pixel chip to flex PCB

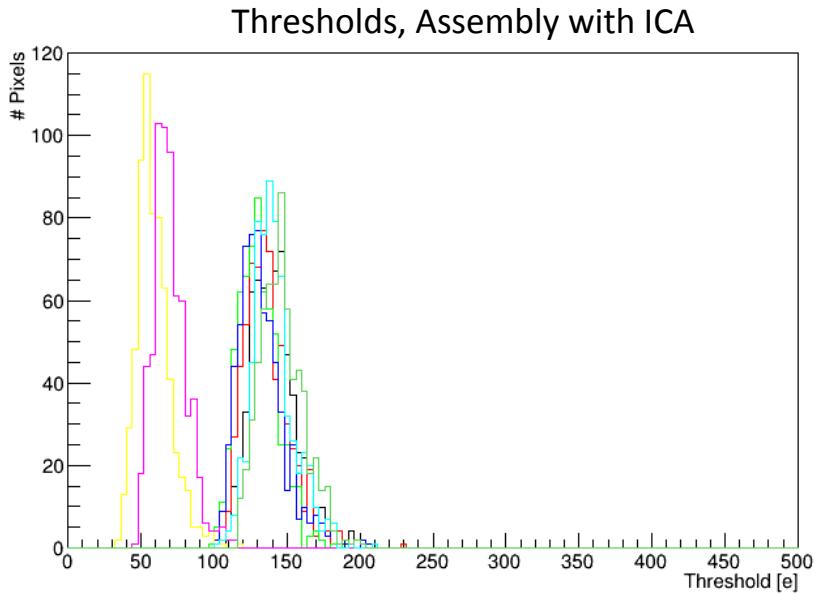
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## Isotropic Conductive Adhesive



## Functional tests



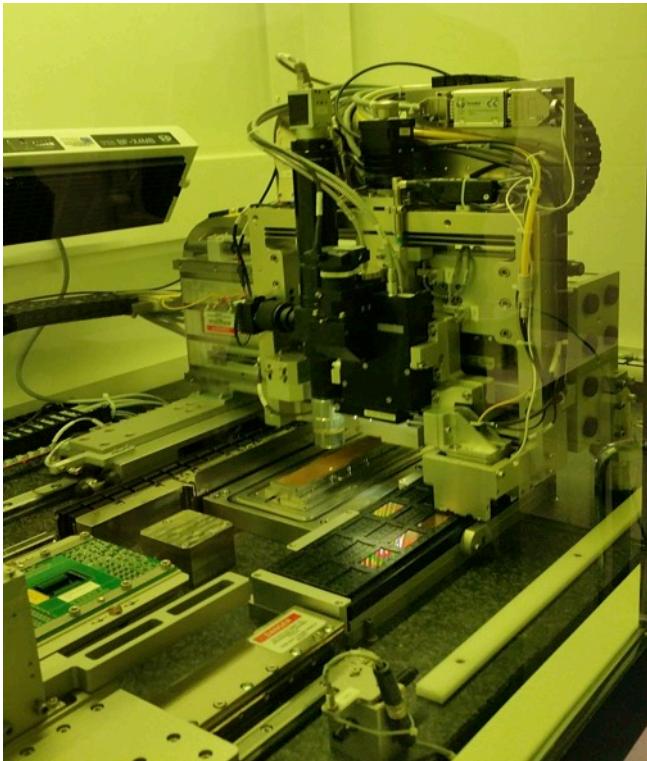
Same results as for wire bonded circuits

Test done after irradiation @ 250 kRad

# Module Assembly Machine

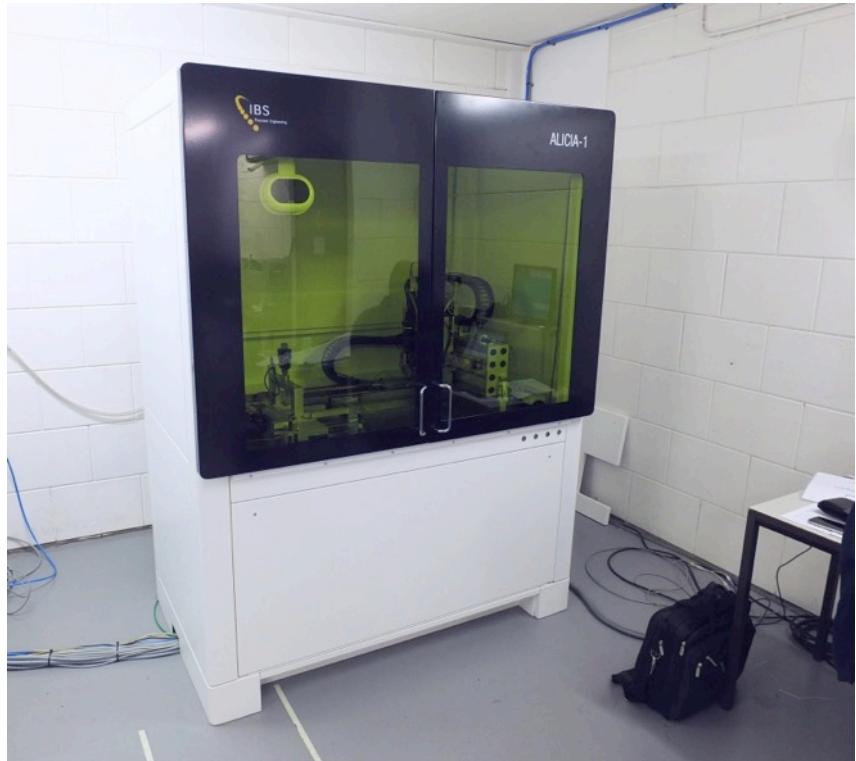
## IB and OB module assembly

- Semi-automatic procedure
- custom machine (specialized company)



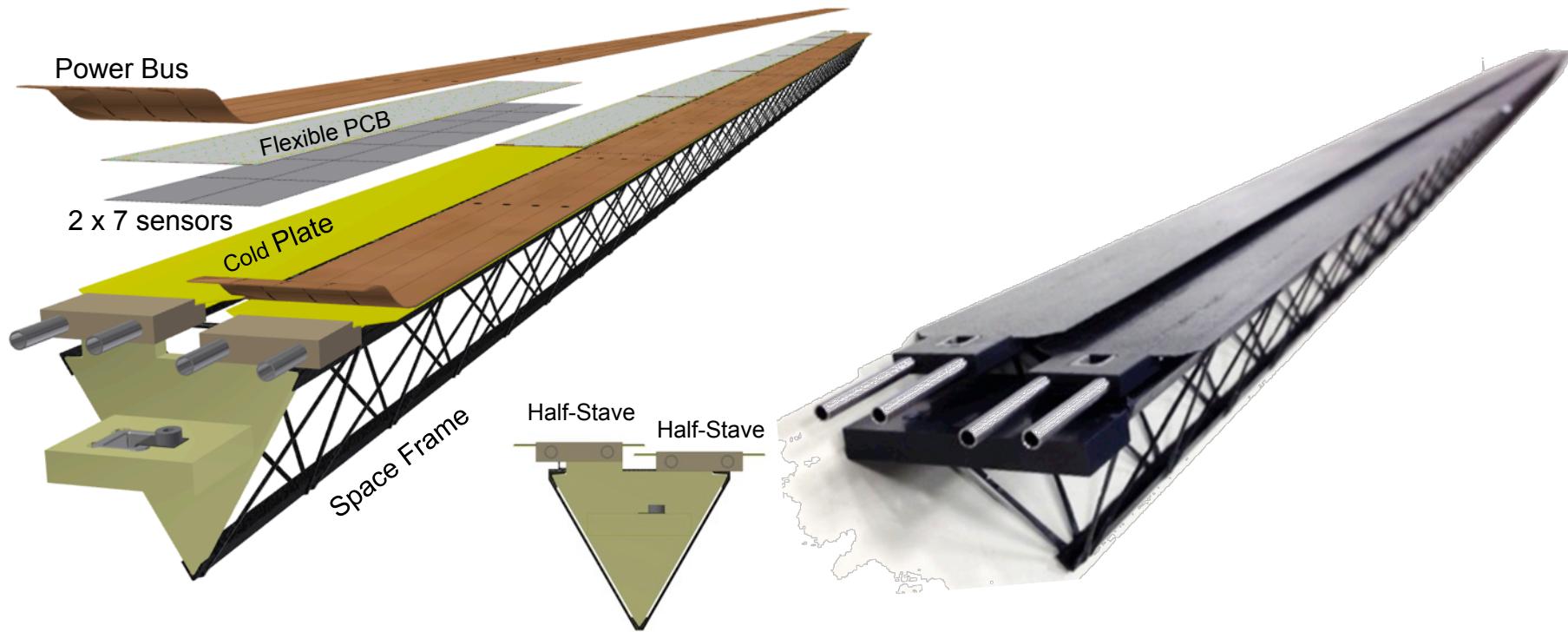
## Status

- Factory Acceptance Test done (March)



## 6 Machines

- Inner Barrel: CERN, Outer Barrel: INFN (Bari), Strasbourg, Liverpool, Pusan, Wuhan
- Same machines used also for chip testing: CERN, Pusan
- Independent machine for chip testing : Yonsei (Seoul)



## Outer Barrel (OB)

$\langle \text{radius} \rangle$  (mm): 194, 247, 353, 405

Nr. staves: 24, 30, 42, 48

Nr. Chips/layer: 6048 (ML), 17740(OL)

Power density < 100 mW / cm<sup>2</sup>

Length (mm): 900 (ML), 1500 (OL)

Nr. modules/stave: 4 (ML), 7 (OL)

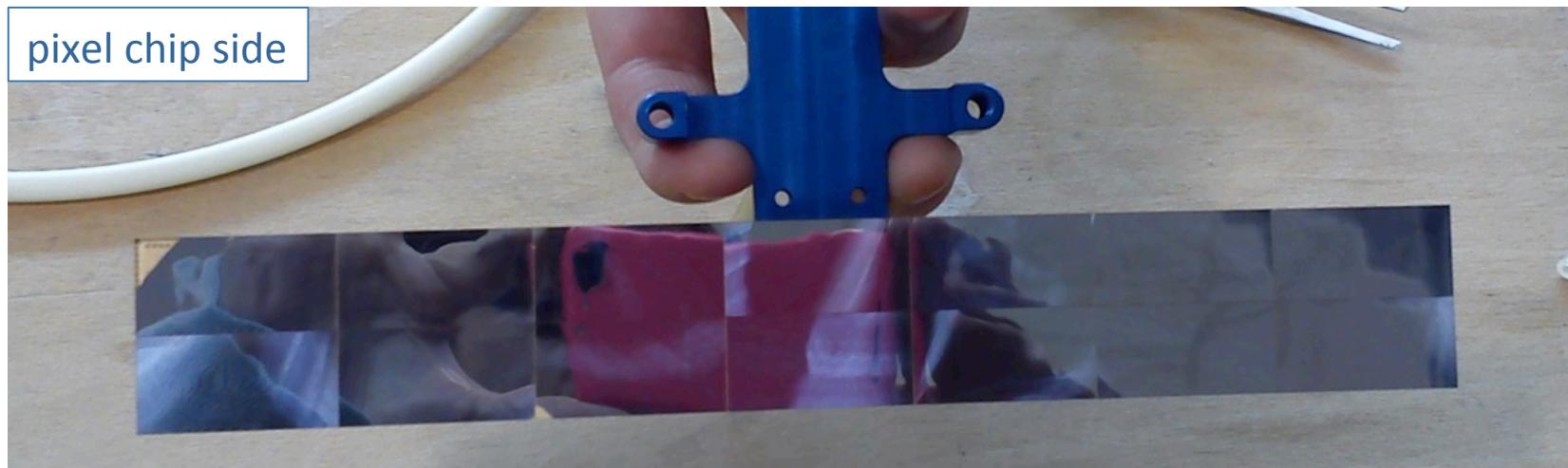
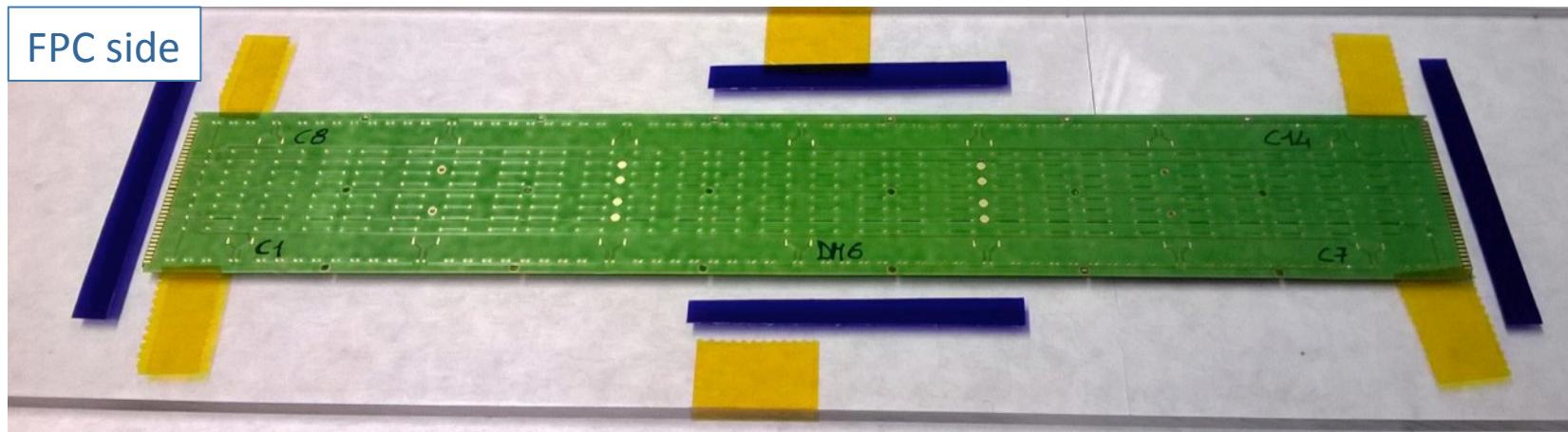
Material thickness:  $\sim 1\% X_0$

Throughput (@100kHz): < 3Mb/s  $\times$  cm<sup>-2</sup>

# ITS Outer Barrel

HIC: Interconnection of pixel chip on flexible printed circuit (FPC)

Bari

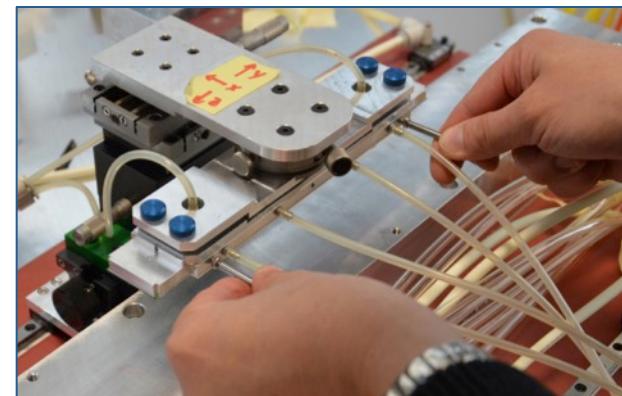
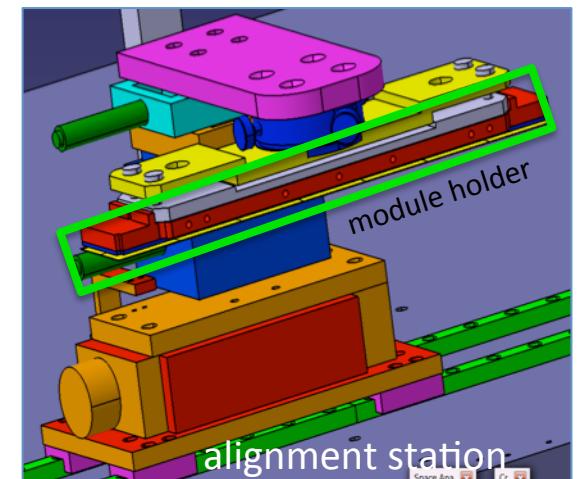
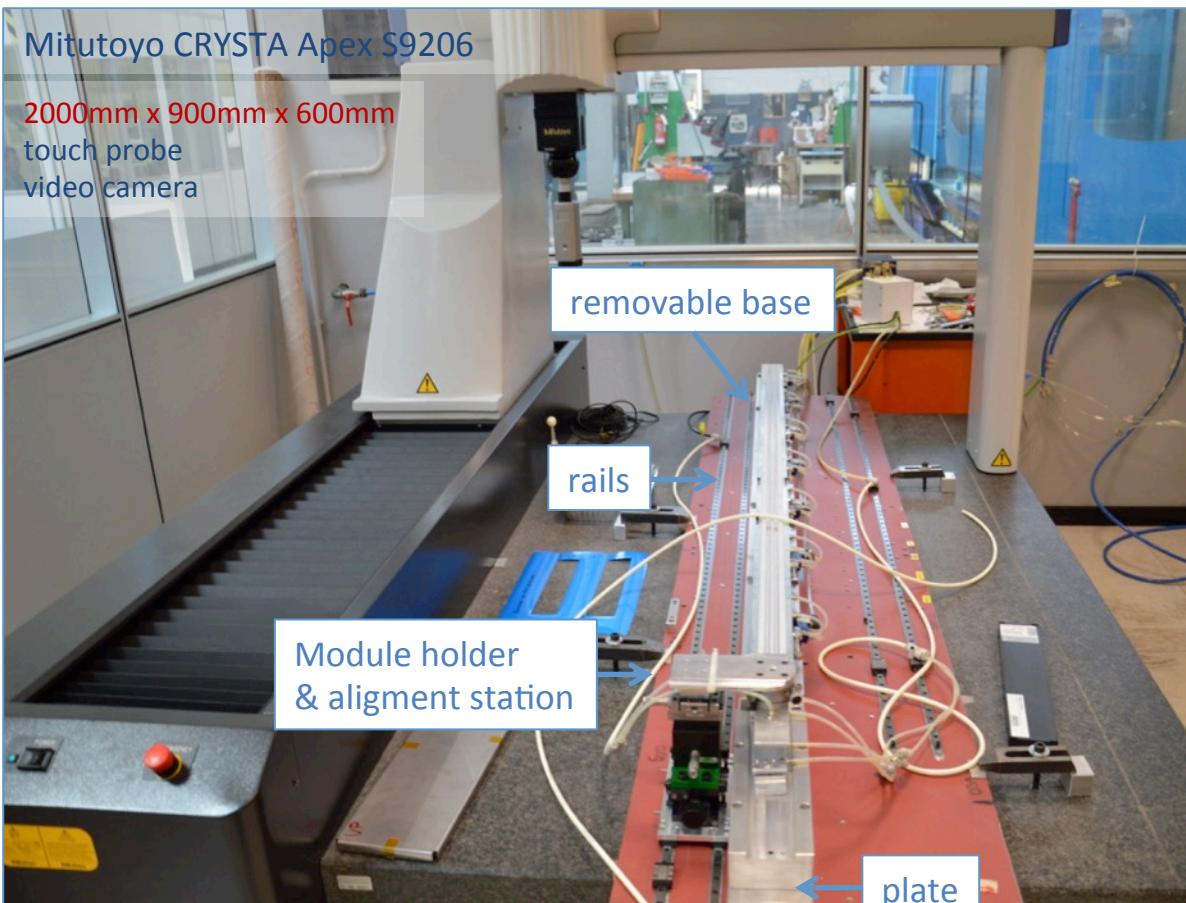


# OB Half Stave – Assembly Jig

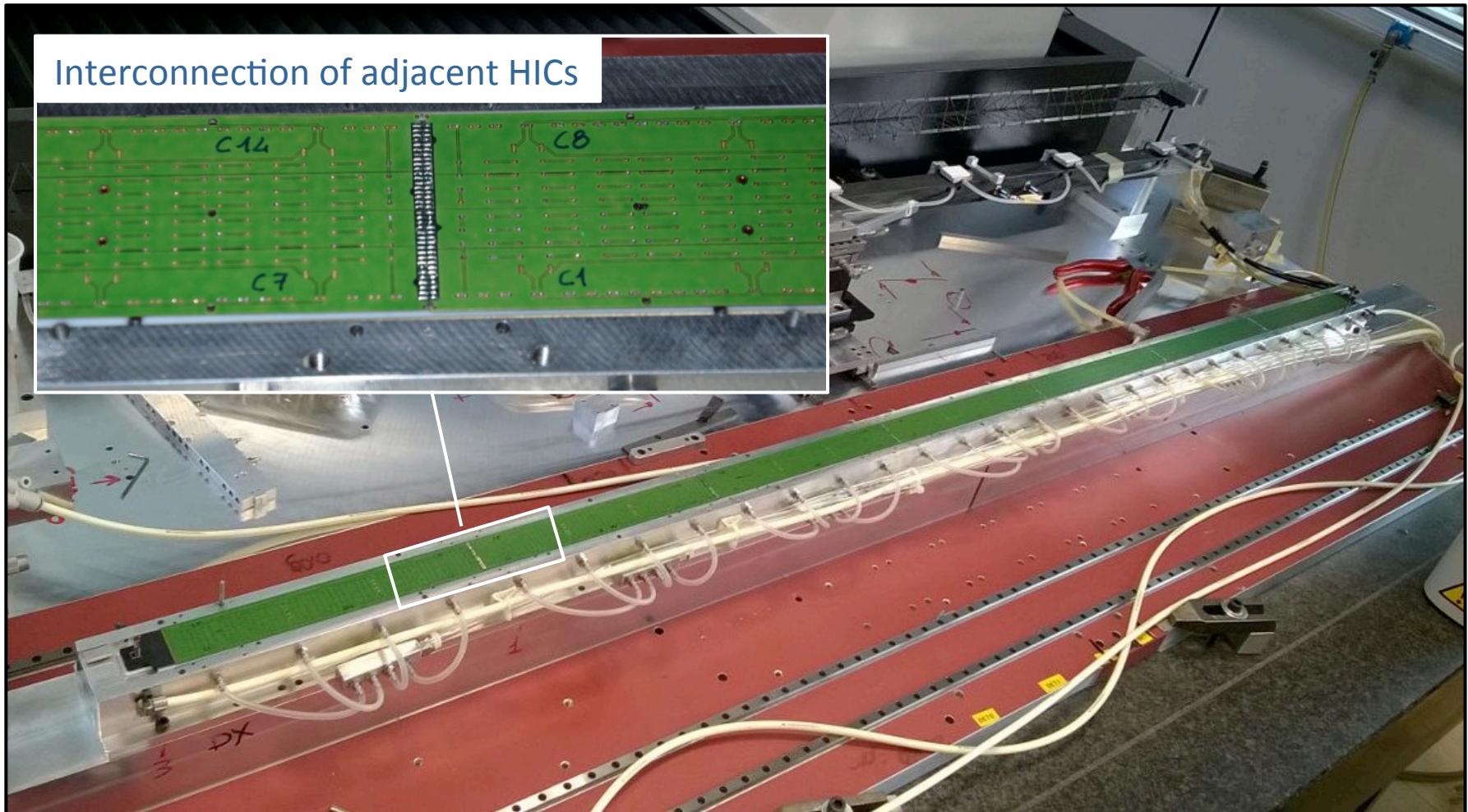
## Main components

- Removable base (vacuum chuck that holds the cold plate)
- Rails to guide the longitudinal movement of the alignment station
- Alignment station
- Module holder

Turin



Half-stave equipped with dummy HICs (dummy silicon chips)



# Stave – Spaceframe & Cold-plate Manufacturing

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Objective: production process optimization

**IB**

## *Pre-series production*

- n. 15 units produced
- n.7 (NA61)



Pre-series production  
well advanced

**OB**



## *Production:*

### Spaceframe

- n.18 units 1.5m (OL) produced
- n.2 units 1.m (ML) produced

Option to procure an oven for spaceframe and coldplate curing process for better control of the temperature uniformity, ( now the heating is by electrical resistance).

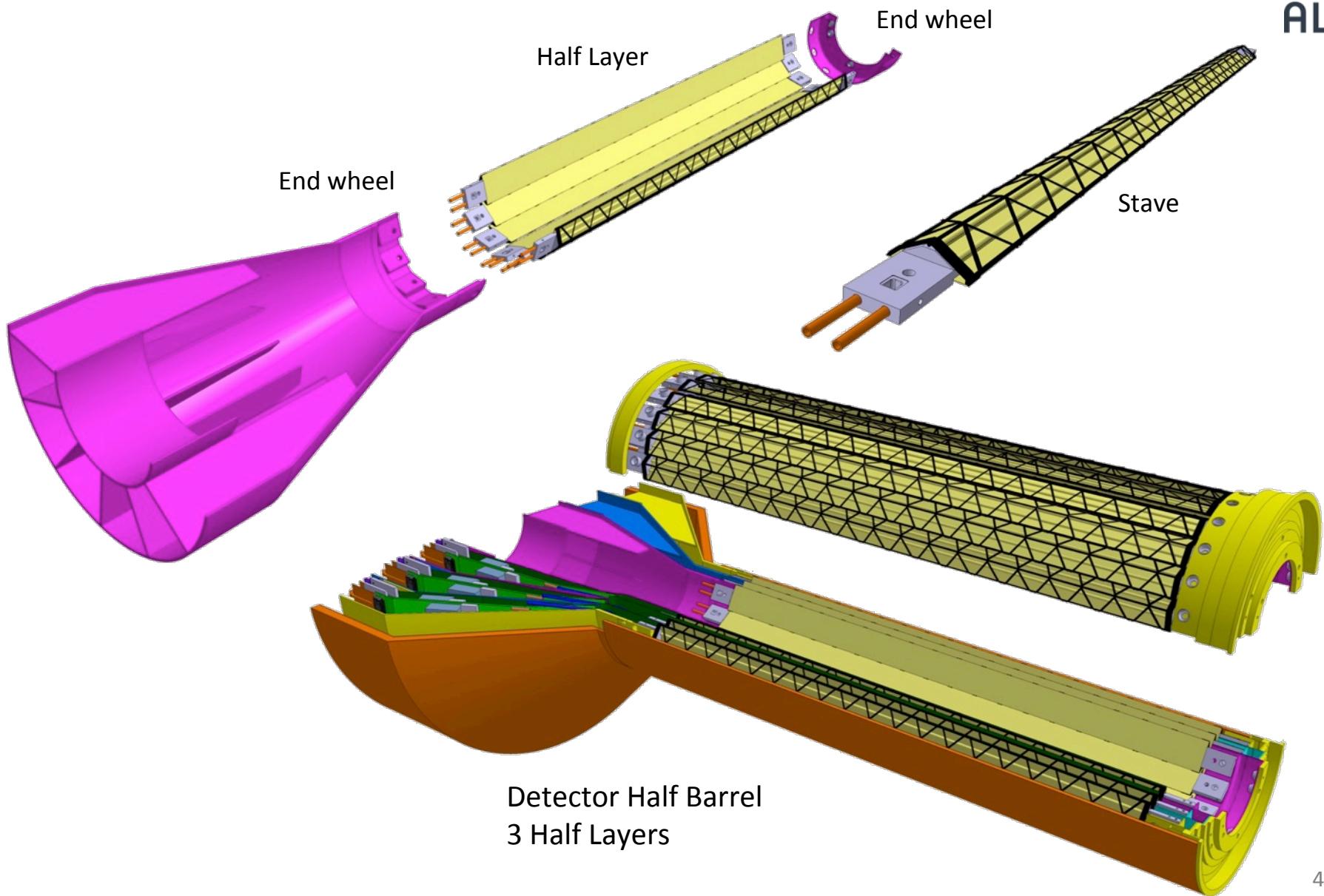
### Coldplate

- n. 4 units 1,5m produced (shipped to INFN TO for dimensional and handling check)
- n.1 unit 1m (ML) produced

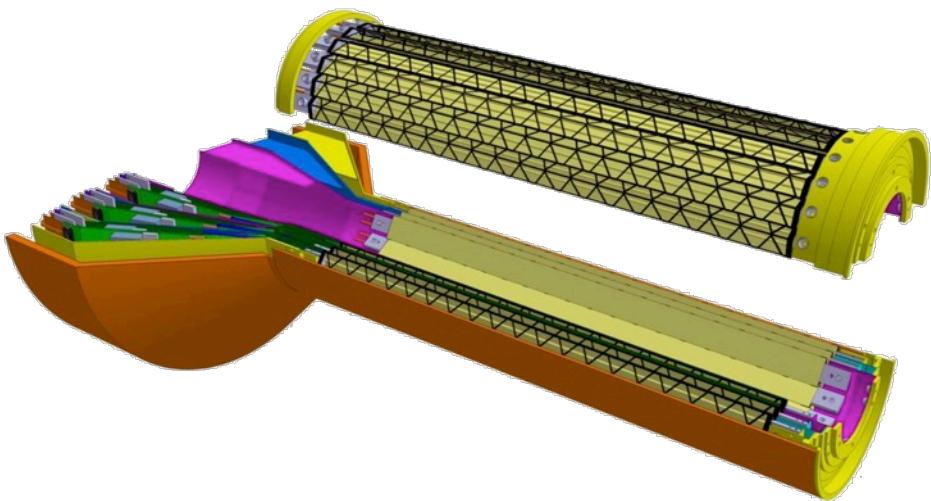
Cold-plate grounding To Be Defined

# Inner Barrel

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# IB End-Wheels



## Mock up

ongoing

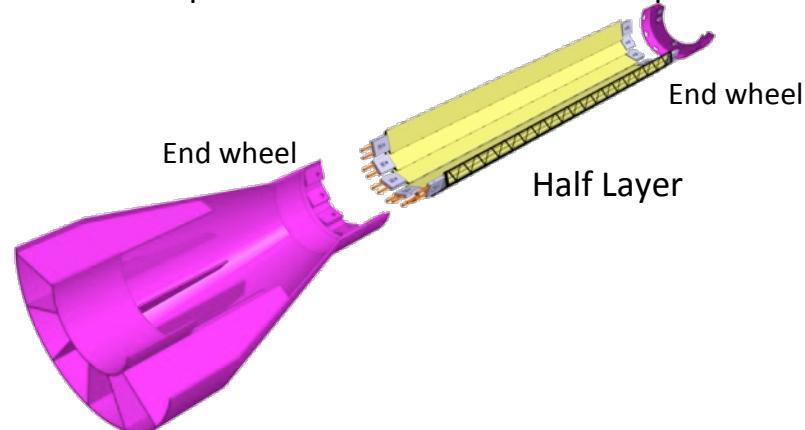
3D printed mock up to verify installation sequence and layout



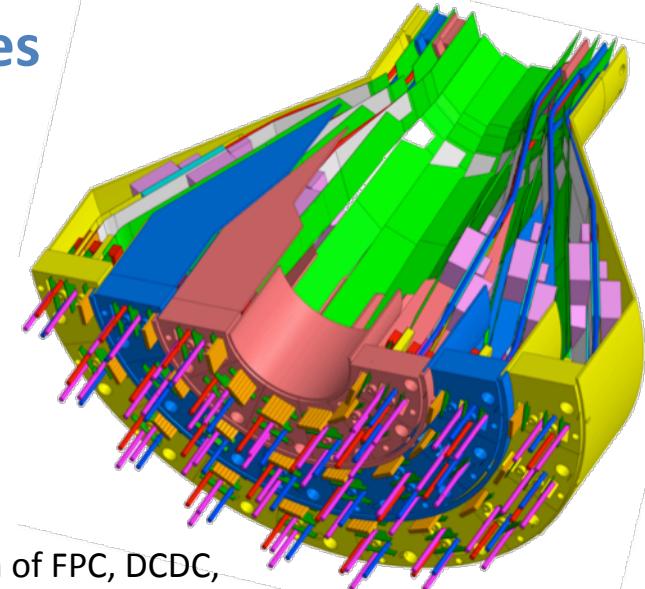
ongoing

Design: FEA to verify stiffness

Material: 3D print Accura Bluestone or Composite



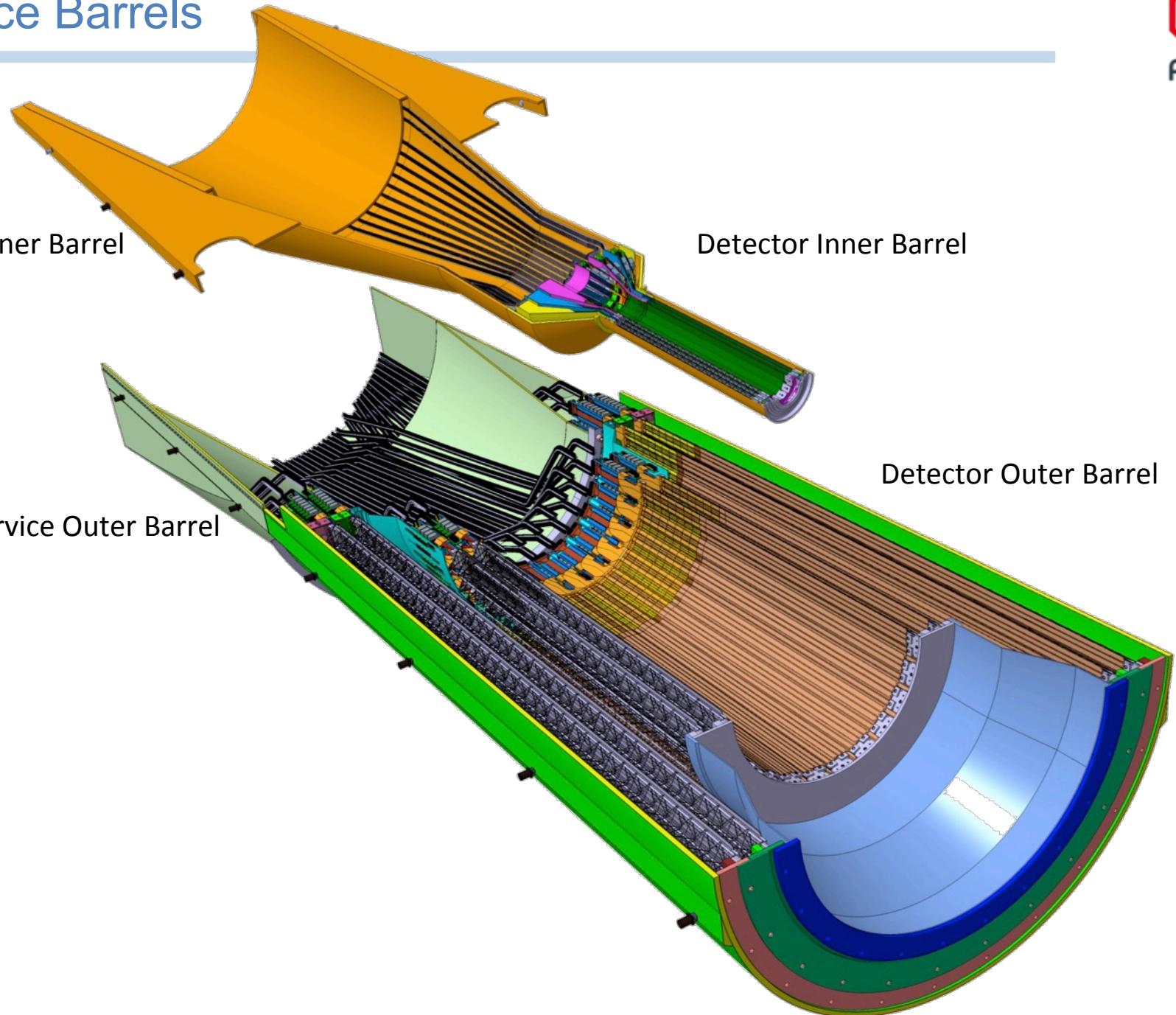
## Services



ongoing

integration of FPC, DCDC,  
power cable, cooling pipes,

# Service Barrels



# Milestones – ALPIDE, IB & OB Staves



A Large Ion Collider Experiment

ITS Master_Plan_V2 (Sep-15)	2015	2016	2017	2018	2019	2020
ALPIDE EDR (10/15)						
ALPIDE PRR (8/16)						
ALPIDE product. and test (end 7/17)						
IB stave EDR (4/16)						
IB stave PRR (8/16)						
IB FPC production end (9/17)						
IB space frame & cold plate prod. end (9/17)						
IB stave production end (1/18)						
IB assembly end (3/18)						
OB stave EDR (4/16)						
OB stave PRR (12/16)						
OB FPC production end (12/17)						
OB space frame & cold plate prod. end (1/18)						
OB HIC production end (4/18)						
OB stave production end (7/18)						
OB stave assembly end (10/18)						

# Milestones – ALPIDE, IB & OB Staves

A Large Ion Collider Experiment



ITS Master_Plan_V2 (Sep-15)	2015	2016	2017	2018	2019	2020
RO electronics EDR (12/16)			😊			
RO electronics PRR (12/17)				😊		
RO electronics prod. end (12/18)					😊	
Detector barrel EDR (7/16)			😊			
Detector barrel PRR (11/16)			😊			
Detector barrel prod. end (7/17)				😊		
Service barrel/cage EDR (9/16)			😊			
Service barrel/cage PRR (2/17)			😊			
Service barrel/cage prod. end (9/17)				😊		
Cooling plant EDR (7/16)			😊			
Cooling plant PRR (10/16)			😊			
Cooling plant ready (9/18)					😊	
Commissioning surface end (5/19)						14 months contingency →
Installation during LS2 (7/20)						← →

# Cost breakdown

A Large Ion Collider Experiment



<b>Activity</b>	<b>Material Costs</b>	<b>Manpower Costs</b>	<b>TOTAL COST / ITEM</b>
<u>1. Pixel Chip</u>	4847	170	5017
1.1 CMOS Wafers	3611		3611
1.2 Thinning & Dicing	800		800
1.3 Series test	436	170	606
<u>2 Inner Barrel</u>	296	262	558
2.1 FPC (construction and test)	23	13	36
2.2 HIC (assembly and test)	250	150	400
2.3 SF & Cold Plate (constr. and test)	3	43	46
2.4 Stave assembly & test	20	56	76
<u>3 Outer Barrel HIC</u>	1447	1118	2565
3.1 FPC (construction and test)	247	88	335
3.2 HIC (assembly and test)	1200	1030	2230
<u>4 Middle Layers Staves</u>	142	322	464
4.1 Powerbus cables	70	3	73
4.2 SF & Cold Plate (constr. and test)	42	113	155
4.3 Stave assembly & test	30	206	236
<u>5 Outer Layers Staves</u>	284	896	1180
5.1 Powerbus cables	127	33	160
5.2 SF & Cold Plate (constr. and test)	97	245	342
5.3 Stave assembly & test	60	618	678

# Cost breakdown

A Large Ion Collider Experiment



Activity	Material Costs	Manpower Costs	TOTAL COST / ITEM
<a href="#"><b>6 Inner Barrel Global Assembly</b></a>	70	156	227
6.1 End-Wheels (E-W)	4	30	34
6.2 Assembly of Staves on E-W	16	12	28
6.3 Cylindrical Structural Shell	1	10	11
6.4 Detector Half-Barrels	6	7	13
6.5 Service Half-Barrels	36	84	120
6.6 Detector + Service Half-Barrels	7	14	21
<a href="#"><b>7 Outer Barrel Global Assembly</b></a>	135	407	542
7.1 ML End-Wheels	13	50	63
7.2 ML Assembly of Staves on E-W	10	21	31
7.3 OL End-Wheels	23	59	82
7.4 OL Assembly of Staves on E-W	12	32	44
7.5 Conical Structural Shell	8	62	70
7.6 Cylindrical Structural Shell	20	55	75
7.7 Detector Half-Barrels	7	13	20
7.8 Service Half-Barrels	36	85	121
7.9 Detector + Service Half-Barrels	7	30	37
<a href="#"><b>8 Integration in ALICE</b></a>	91	262	354
8.1 Cage	61	153	215
8.2 Installation Tooling	30	109	139

# Cost breakdown

A Large Ion Collider Experiment



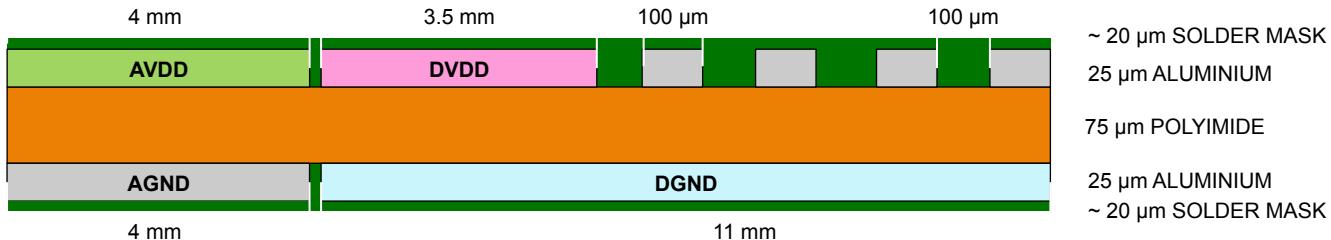
Activity	Material Costs	Manpower Costs	TOTAL COST / ITEM
<u>9 Readout Electronics</u>	715	50	765
9.1 Data e-Links	82	50	132
9.2 Patch-panels	20		20
9.3 Readout Unit	469		469
9.4 Optical Links	144		144
<u>10 Power distribution</u>	1149	50	1199
10.1 Power Supplies	750		750
10.2 Power Distribution	242	50	292
10.3 Power Regulation	157		157
<u>11. DCS</u>	150		150
<u>12. Cooling</u>	620	0	620
12.1 Water Cooling Plant	470		470
12.2 Ventilation Humidity Plant	150		150
<b>GRAND TOTAL</b>	<b>9947</b>	<b>3693</b>	<b>13640</b>

# Spare Material

# Inner Barrel Stave – flexible printed circuit

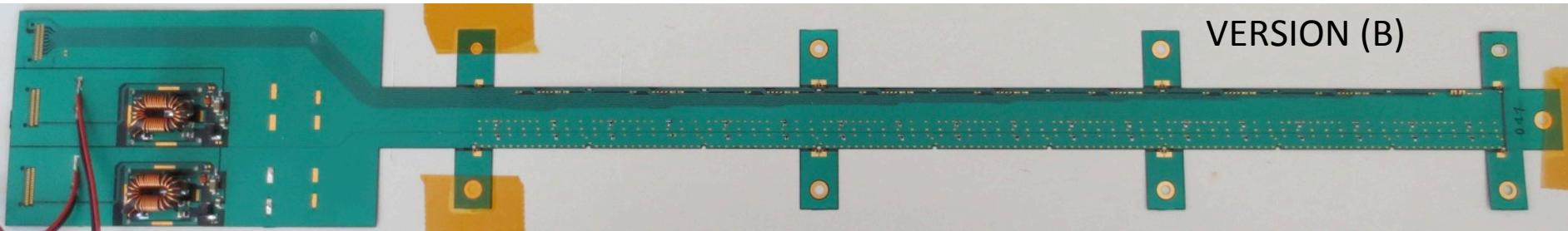
## IB Flexible Printed Circuit prototypes (Al power planes and signal tracks)

Metallised vias of  
220 $\mu$ m diameter



### Status

Two FPC versions (differ for the location of DC-DC converters)  
ready to be tested with ALPIDE-2

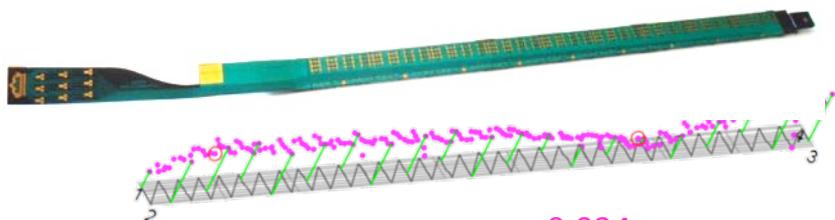


# Inner Barrel Stave



## Stave HIC+ Space frame assembly

Dimensional accuracy



+0.034 mm  
- 0.034 mm

### status

New master jig ([ready](#)) will improve stave accuracy

## Space frame production

### status

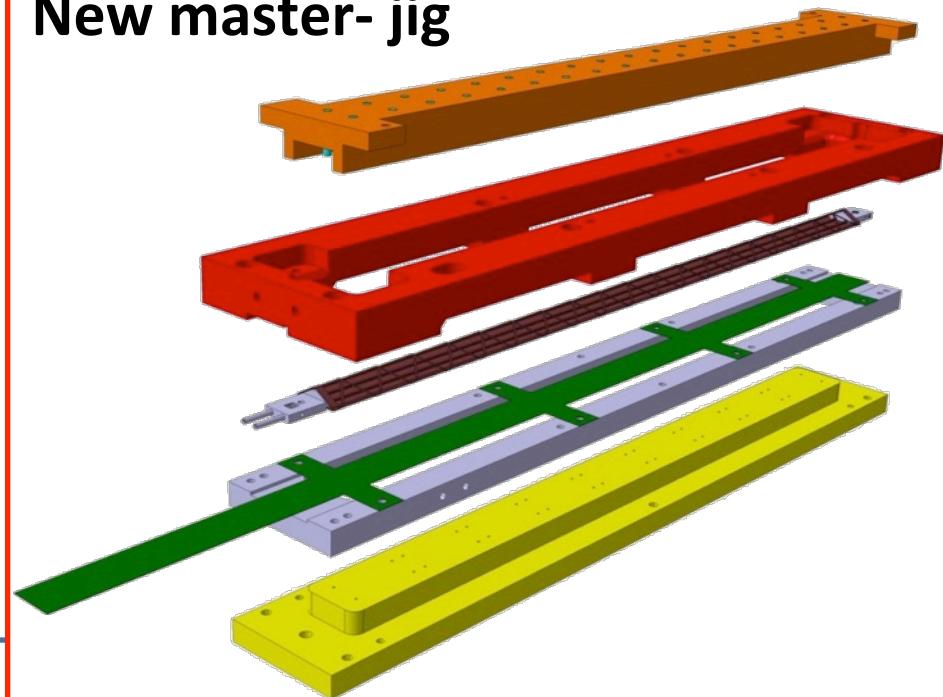
Available : n. 20 spaceframe

### Ongoing

pre-production continues to prepare for final series production



## New master- jig

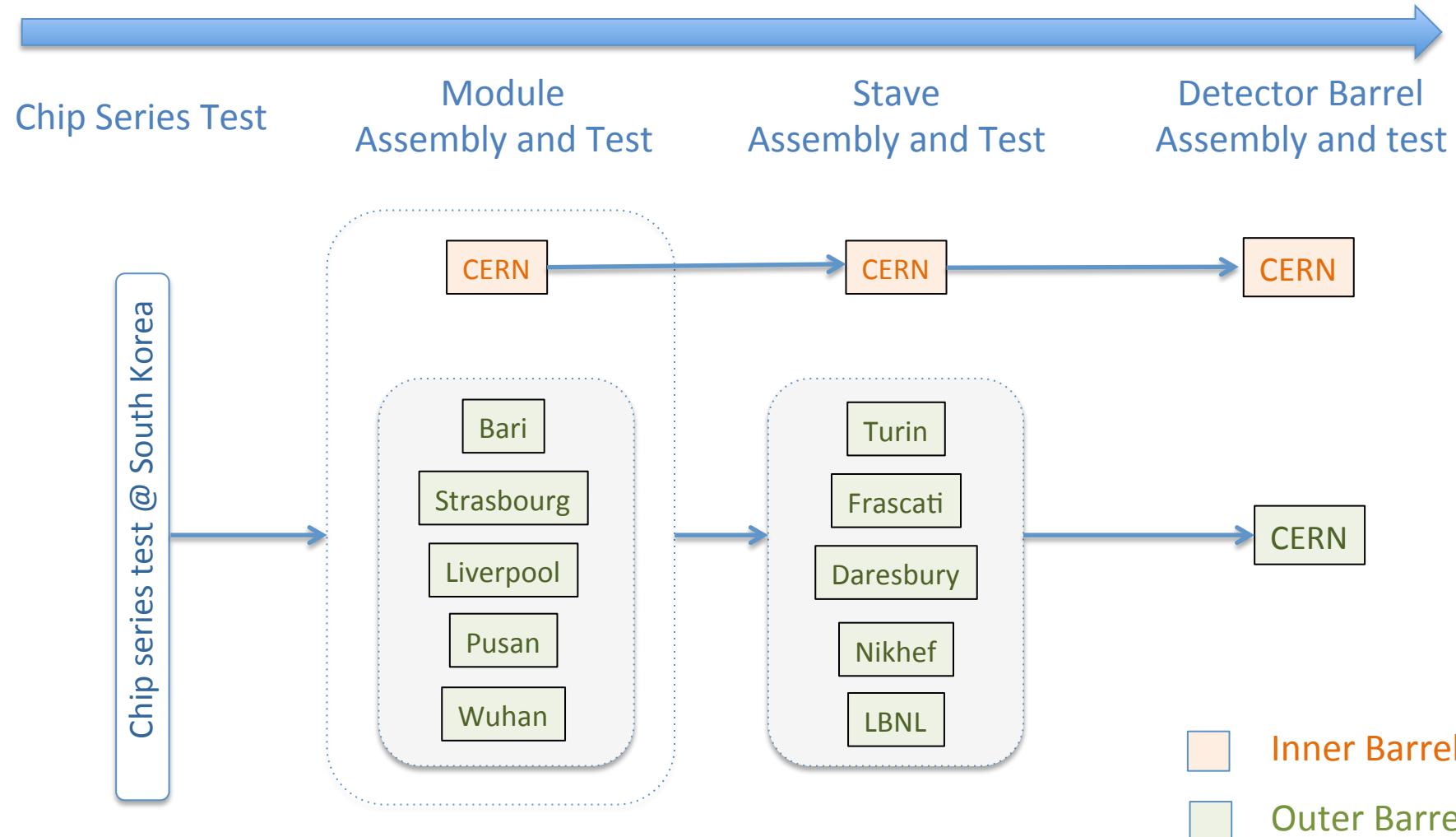


### ongoing

New master jig produced and shipped from the Company,  
metrological verification ongoing

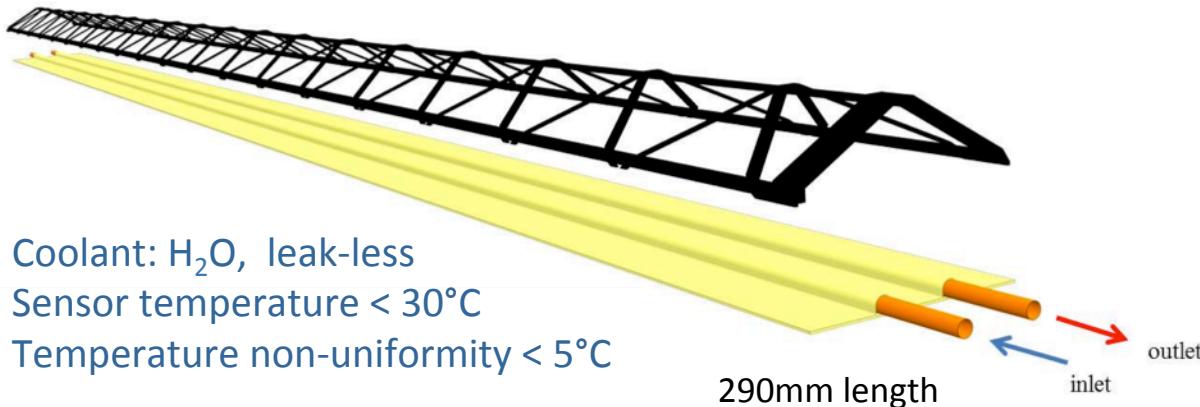
Layout and curing process optimization: planarity achieved  
 $\pm 0,028 \div 0,040$  mm

# Module and Stave production flow chart

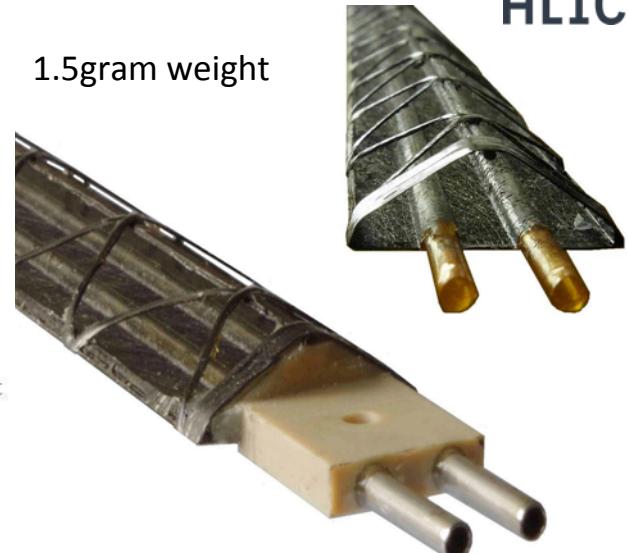


# Inner Barrel – Geometry and material budget

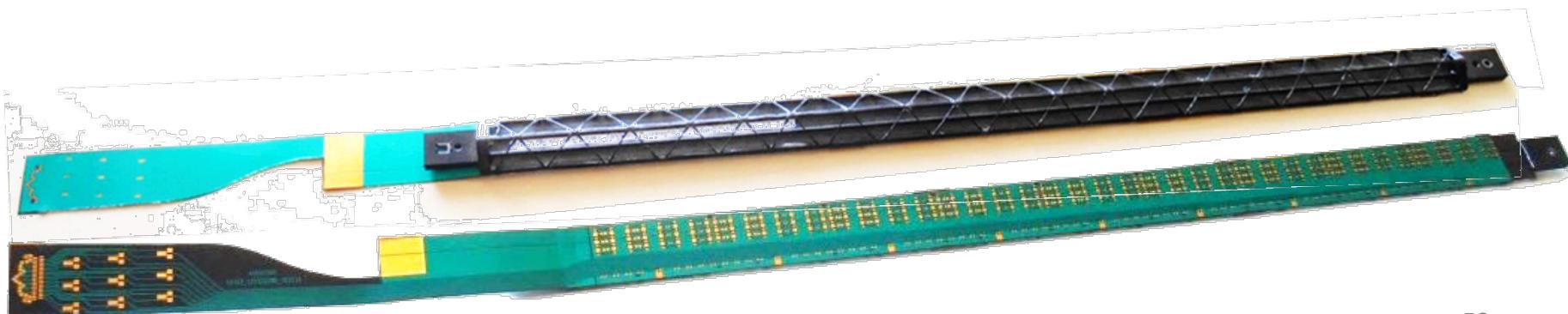
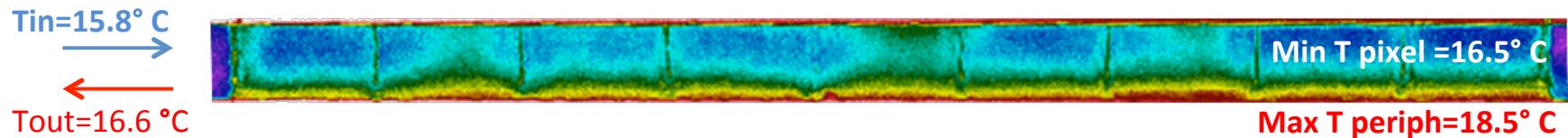
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1.5gram weight



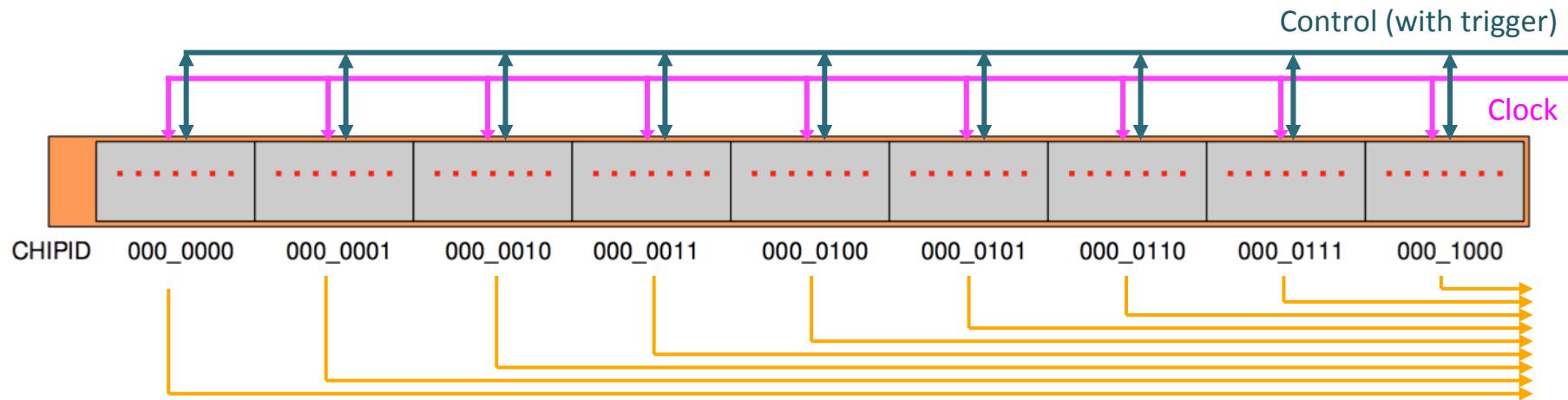
$$W = 100 \text{ mW / cm}^2 (\text{> x2 nominal}), \text{ H}_2\text{O flow rate} = 3 \text{ Lh}^{-1}$$



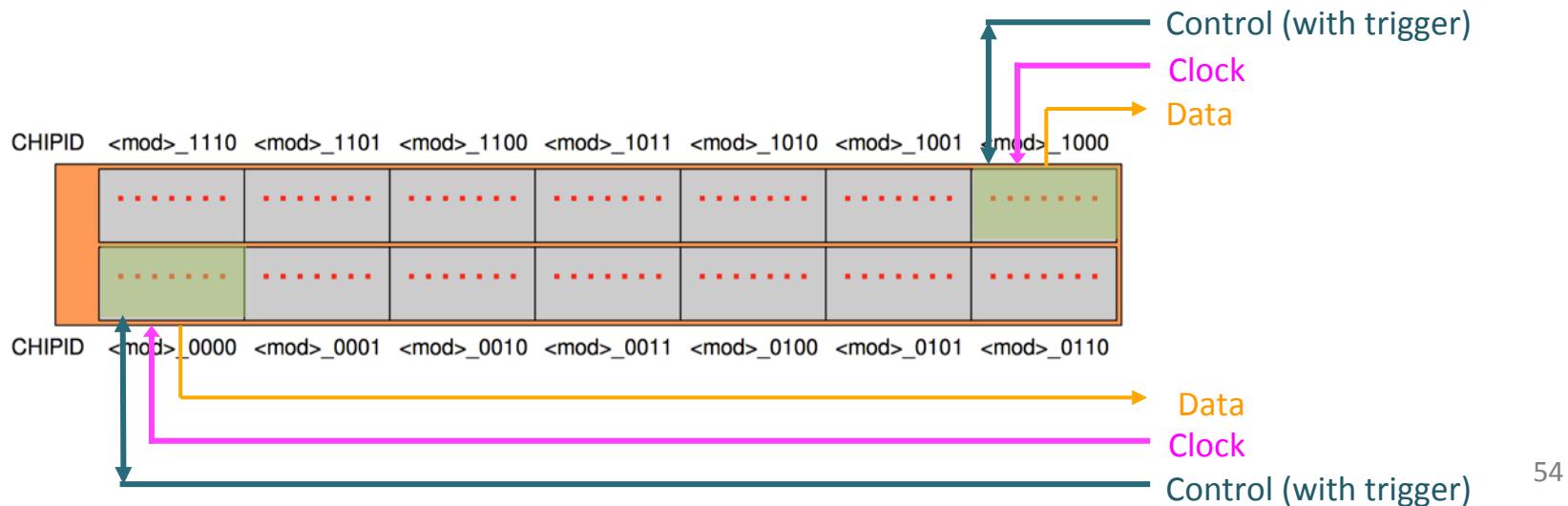
# Readout – Inner and Middle/Outer Layers connections

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**Inner layers stave**, 9 independent sensors (each read/drives its own data lines)



**Mid/Outer layers module**: 2 symmetric group of 1 master and 6 slave chips. Only the master accesses the data/control lines toward/from the outer world.



# Readout – copper links and available bandwidth

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Inner layers (0, 1, 2) staves:  
9 masters for each stave

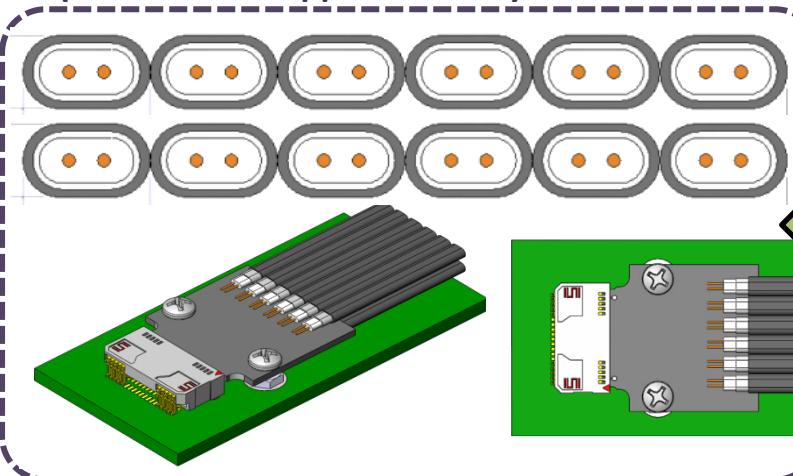


≈ 30 cm

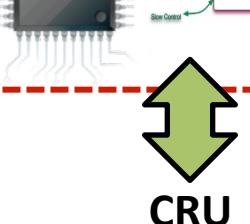
≈ 5m

9 copper pairs,  
1.2 Gb/s each

12 pairs Twinax copper assembly



Readout Unit



Mid layers (3, 4) staves: 8 modules per stave, 2 master each

MODID = 001

MODID = 010

MODID = 011

MODID = 100

MODID = 001

MODID = 010

MODID = 011

MODID = 100

≈ 80 cm

16 copper pairs,  
400 Mb/s each

≈ 5m

28 copper pairs,  
400 Mb/s each

≈ 5m

Outer layers (5, 6) staves: 14 modules per stave, 2 master each

MODID = 001

MODID = 010

MODID = 011

MODID = 100

MODID = 101

MODID = 110

MODID = 111

MODID = 001

MODID = 010

MODID = 011

MODID = 100

MODID = 101

MODID = 110

MODID = 111

≈ 150 cm

# Readout – general scheme

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